Points missed: _____ Student's Name: _____

Total score: _____/100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 2 for Fall Semester, 2005

Section 001

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes.
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- ***Calculators are not allowed.*** Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

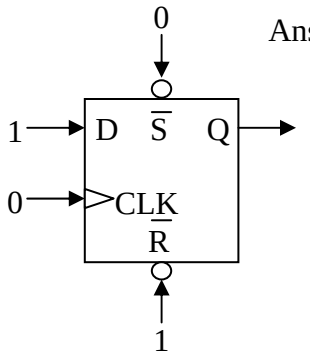
"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

Short answers – 2 points each

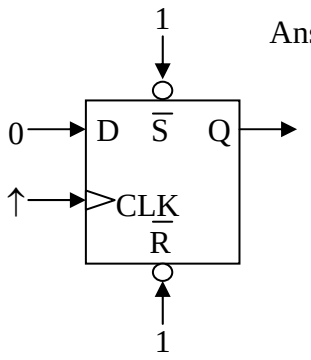
For the following ***four*** circuits, identify the value of the output Q from the following choices. Consider the D-latch a rising edge triggered latch.

a.) 1 b.) 0 c.) Q_0 (stored value of Q) d.) Q_0 (inverse of stored value of Q) e.) undefined

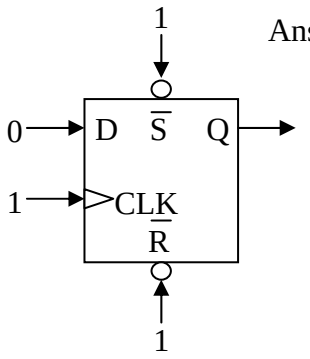
1. Answer: a



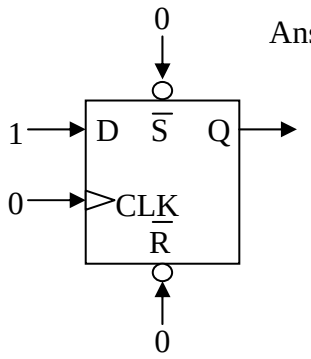
2. Answer: b



3. Answer: c



4. Answer: e



5. The expression $\bar{A}\cdot B\cdot C + A\cdot B\cdot C + \overline{A\cdot B}$ is not in proper Sum-of-Products format. What boolean algebra operation would you need to apply to correct this?

   a.) It's not a problem; illegal term drops out b.) Distributive Law c.) Use "F-O-I-L"
   d.) Take the inverse of the inverse e.) DeMorgan's Theorem f.) It can't be fixed

6. True or False: There exists exactly one pattern of rectangles for every pattern of 1's and 0's in a Karnaugh map.

   All it takes is finding one case where this isn't true. The following is one of those cases. (Note the red rectangle.)

AB \ CD	00	01	11	10
00	0	1	1	0
01	0	0	1	0
11	0	0	1	1
10	0	0	0	0

AB \ CD	00	01	11	10
00	0	1	1	0
01	0	0	1	0
11	0	0	1	1
10	0	0	0	0

7. True or False: In a Karnaugh map, there must be an adjacent cell for every possible single-variable change. For example, if a Karnaugh map has three input variables, then there must be three cells adjacent to every cell in the map where only one variable value changes in a move to that cell.

   This is true. Remember that the purpose of a Karnaugh map is to rearrange the truth table so that adjacent cells can be combined allowing for a term to drop out. In other words, the key to the effectiveness of Karnaugh maps is that each cell represents the output for a specific pattern of ones and zeros at the input, and that to move to an adjacent cell, exactly one of those inputs can change, the rest must remain the same. Take for instance the 16 cell (4-input) Karnaugh map. The cell in the third column of the second row represents the condition where A=0, B=1, C=1, and D=1. Moving to the cell immediately to the left will change only C; moving right will change D; moving up changes B; and moving down changes A. Therefore, there is an adjacent cell that represents a change in any of the four input variables.

8. How many cells does a 3 input Karnaugh map have?

   a.) 4 b.) 6 c.) 8 d.) 16 e.) 24 f.) 32

9. In a 4-variable Karnaugh map, how many input variables (A, B, C, or D) does a product have if its corresponding rectangle of 1's contains 2 cells?

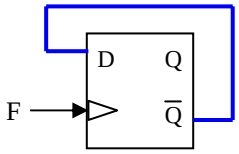
   a.) 1 b.) 2 c.) 3 d.) 4 e.) Cannot be determined

10. A falling edge triggered latch copies data from the D input to the Q output when the clock is:

    a.) a logic 0 b.) changing from a 1 to a 0 c.) a logic 1 d.) changing from a 0 to a 1

11. True or False: Both the $\overline{S}$ and $\overline{R}$ inputs to a D-latch have priority over the D and clock inputs.

12. Make the connections to the latch in the figure to the right that makes a divide-by-two circuit, i.e., divides the frequency F in half at the output Q.



13. Which of the following sums produces the truth table to the right?

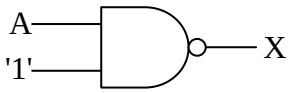
    a.) $A+B+\overline{C}$ b.) $\overline{A}+\overline{B}+C$ c.) $\overline{A}+B+\overline{C}$

    c.) $\overline{B}+C$ d.) $B+\overline{C}$ d.) None of the above

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

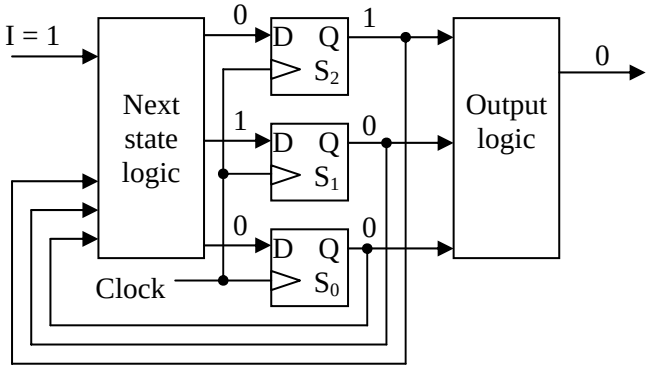
   Going back to our original discussion of POS circuits, we know that we need to create a sum for each of the rows where a zero appears in the truth table. For the row where A=0, B=0, and C=1, the corresponding sum is $A+B+\overline{C}$. For the row where A=1, B=0, and C=1, the corresponding sum is $\overline{A}+B+\overline{C}$. When we combine these two sums, we see that the circuit is to output a 0 if B=0 and C=1 and A can equal either 0 or 1 (and hence drops out of the expression). Therefore, the answer is D.

14. Fill in the truth table for the NAND circuit shown below.



A	X
0	1
1	0

The next four problems use the state machine diagram to the right. Assume that the states are numbered so that bit S_2 is the MSB and bit S_0 is the LSB.



15. What is the maximum number of states that this system can handle?

Since there are three latches, then the internal memory of this state machine can remember 8 states: 000, 001, 010, 011, 100, 101, 110, and 111. Therefore, the answer is 8.

16. True or false: If the input I changed from 1 to 0, but everything else remained unchanged, the output of the system would remain unchanged.

The output of the type of state machine we've described in class relies ONLY on the current state. Since only the input is changing (i.e., we don't get a clock pulse to move to the next state) then the current state stays the same and so does the output.

17. What is the current state of this system? Keep your answer in binary.

The current state is the value stored in the latches. In the case of the diagram above, that is 1-0-0 with S_2 being the most significant bit.

18. If the clock were to pulse right now, what would the next state be? Keep your answer in binary.

A clock pulse will take the values at the inputs of the latches and store them. This will change the current state to the values at the latch inputs, i.e., 0-1-0.

19. True or False: Renumbering the states of a state machine has no effect on the "next state" logic for the digital hardware implementation.

The numbering of the states directly affects the next state truth table, and therefore changes the logic that is derived from it. Therefore, the answer is **False**.

20. How many latches will a state machine with 22 states require?

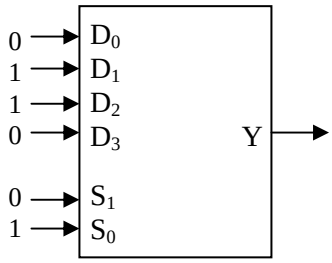
a.) 1 b.) 2 c.) 3 d.) 4 e.) 5 f.) 6 g.) 7

Twenty-two states will be numbered 0, 1, 2, 3, … , 20, and 21. Since $21_{10} = 10101_2$, we will need 5 bits to represent the state. **Therefore, the answer is e.** Another way of looking at it is to see how many states it is possible to represent with n bits, and to figure out what value of 2^n is greater than or equal to 22. $2^4 = 16$ which is not enough, but $2^5=32$. Therefore, 5 bits will do the trick.

21. If a group of four rows or columns in a Karnaugh map is identified with two variables, it is numbered 00, 01, 11, 10 instead of 00, 01, 10, 11. Why?

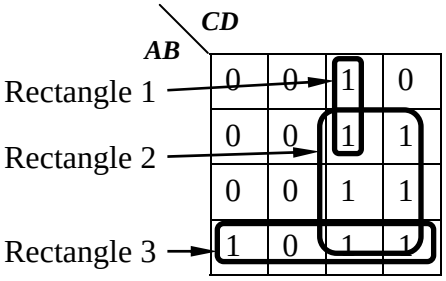
Because any horizontal or vertical movement between adjacent cells can only have 1 input variable change. Numbering 00, 01, 10, 11 has two variables changing when going from 01 to 10 and when wrapping around the table from 00 to 11. 00, 01, 11, 10 does not have this problem.

22. For the multiplexer/selector shown to the right, what is the output Y?



Remember that a multiplexer is like a digitally controlled channel changer using the inputs S_1 and S_0, to select either D_0, D_1, D_2, or D_3 to be output to Y. The way it works is that the decimal equivalent of the bits at the inputs S_1 and S_0 identify the subscript of the D input being routed to Y. Since S_1 and S_0 equal 0 and 1 respectively, and since $01_2 = 1_{10}$, then D_1 is routed to Y. Since D_1 equals 1, then the output at Y equals 1.

23. For the Karnaugh map to the right, identify the problems with each of the three rectangles shown. (2 points each)



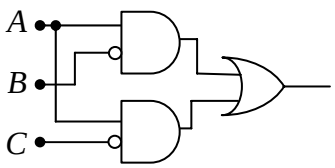
Rectangle 1: This rectangle could be made larger by doubling it downward to include the whole column.

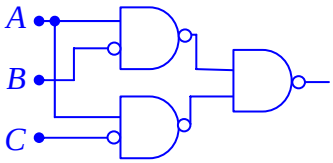
Rectangle 2: This rectangle encloses a non-power of 2 number of cells, specifically 6.

Rectangle 3: This rectangle contains a zero.

Medium answers – 4 points each

24. Convert the Sum-of_Products circuit shown below to NAND-NAND logic, i.e., a circuit that contains nothing but NAND gates (and possible inverters at inputs).

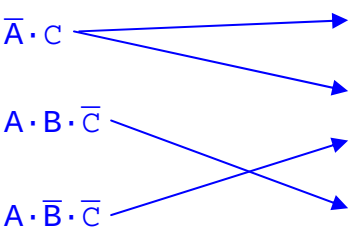




25. Complete the truth table to the right with the values for the following Sum-of-Products expression:

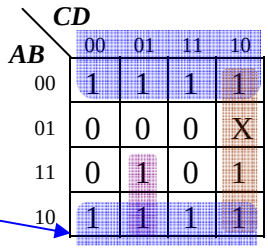
$$X = (\overline{A} \cdot C) + (A \cdot B \cdot \overline{C}) + (A \cdot \overline{B} \cdot \overline{C})$$

Remember that each product generates one's in the truth table for the case where 1·1·1 = 1.



A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

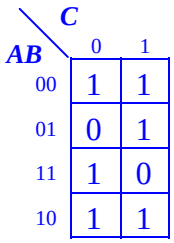
26. In the Karnaugh map to the right, draw the best pattern of rectangles you can. ***Do not derive the SOP expression.***



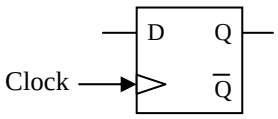
Connects with other half of rectangle on top of K-map.

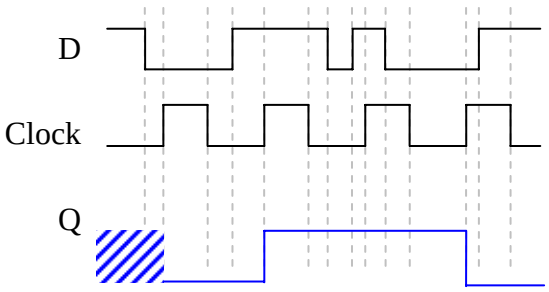
27. Create a Karnaugh map from the truth table below. ***Do not worry about making the rectangles.***

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



28. Show the *D* latch output waveform *Q* based on the inputs *D*, $\overline{S}$, $\overline{R}$, and clock indicated in the graph to the right. Assume the latch captures on the rising edge. (The figure below is just for a reference.)



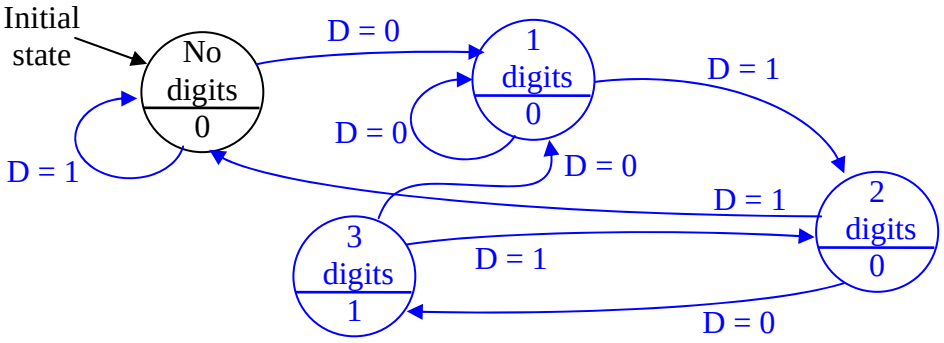


Longer answers – Points vary per problem

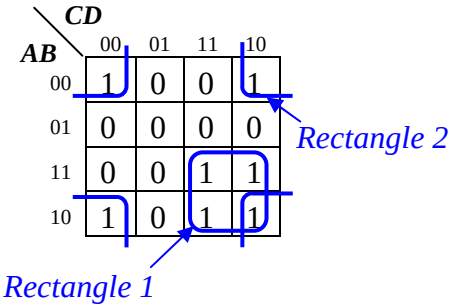
29. Make the state diagram that will output a '1' when the sequence '010' is detected in a serial stream of bits. For example, if the following binary stream is received:

0 0 0 1 0 1 1 1 1 0 0 1 0 1 0 0 0 0 1 1 1 0 1 0 0 0 1 1

then 1's will be output here. (Notice that the last zero of the second pattern is shared with the first zero of the third pattern.) At all other times, the system will output zeros. Label the input D. (8 points)



30. Derive the minimum SOP expression from the Karnaugh map below. (6 points)



Rectangle 1

A	B	C	D
1	1	1	1
1	1	1	0
1	0	1	1
1	0	1	0

B and D drop out. Since A & C are 1, neither is inverted.

$A \cdot C$

Rectangle 2

A	B	C	D
0	0	0	0
0	0	1	0
1	0	0	0
1	0	1	0

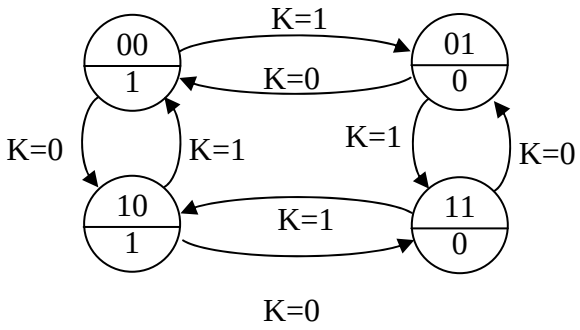
A and C drop out. B & D are both 0, so both are inverted.

$\overline{B} \cdot \overline{D}$

The final answer is:

$A \cdot C + \overline{B} \cdot \overline{D}$

31. Create the next state truth table and the output truth table for the state diagram to the right. Use the variable names S_1 and S_0 to represent the most significant and least significant bits respectively of the binary number identifying the state. Label the output 'X'. (8 points)



Next State T.T.

S_1	S_0	K	S_1'	S_0'
0	0	0	1	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	1
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

Output T.T.

S_1	S_0	X
0	0	1
0	1	0
1	0	1
1	1	0

32. The three Boolean expressions below represent the ***next state bits (S_0' and S_1')*** and the ***output bit X*** based on the ***current state (S_0 and S_1)*** and the ***input A***. Draw the logic circuit for the state machine including the latches and output circuitry. ***Be sure to label the latch inputs and other signals.***
(8 points)

$S_0' = \overline{S_1} \cdot A$ $\quad$ $S_1' = \overline{S_0} \cdot A$ $\quad$ $X = S_1 \cdot \overline{S_0}$