Points missed: _____   Student's Name: _____

Total score: _____ /100 points

Section 001

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes.
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- *Calculators are not allowed.* Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

Binary	Hex		Binary	Hex		Power of 2	Equals
0000	0		1000	8		2^3	8
0001	1		1001	9		2^4	16
0010	2		1010	A		2^5	32
0011	3		1011	B		2^6	64
0100	4		1100	C		2^7	128
0101	5		1101	D		2^8	256
0110	6		1110	E		2^9	512
0111	7		1111	F		2^{10}	1K

"Fine print"

1. How many cells total does a 3 variable Karnaugh map have? (2 points)

   A three variable K-map has the same number of cells as a three variable truth table has row. This represents the total number of combinations of 1's and 0's for three variables: $2^3=8$.

2. In a 4-variable Karnaugh map, how many variables (e.g., A, B, C, etc.) does a product have if its rectangle of 1's contains 4 cells? (2 points)

   Remember that each time the size of a rectangle is doubled (e.g., 1 cell doubled to 2 cells, 2 cells doubled to 4 cells, etc.) a single input variable drops out. In addition, a rectangle of size 1 uses all of the input variables. Therefore, since a rectangle of 4 cells has doubled twice over the size of a single cell rectangle, there are 2 variables that have dropped out. *Therefore, a product from a rectangle of four cells in a 4-variable K-map has 2 variables.*

3. If a group of four rows or columns in a Karnaugh map is identified with two variables, it is numbered 00, 01, 11, 10 instead of 00, 01, 10, 11. Why? (4 points)

   Because any horizontal or vertical movement between adjacent cells can only have 1 input variable change. Numbering 00, 01, 10, 11 has two variables changing when going from 01 to 10 and when wrapping around the table from 00 to 11.

4. Create a Karnaugh map from the truth table below. Do not worry about making the rectangles. (5 points)

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

C
AB	0	1
00	0	0
01	1	0
11	1	1
10	1	0

5. Derive the minimum SOP expression from the Karnaugh map below. (6 points)

CD \ AB	00	01	11	10
00	1	0	1	1
01	0	0	1	0
11	0	1	1	0
10	0	1	1	0

Rectangle 1

A	B	C	D
0	0	0	0
0	0	1	0

C drops out and A, B, and D are inverted.

$\overline{A} \cdot \overline{B} \cdot \overline{D}$

Rectangle 2

A	B	C	D
1	1	0	1
1	1	1	1
1	0	0	1
1	0	1	1

B and C drop out and A and D are not inverted.

$A \cdot D$

Rectangle 3

A	B	C	D
0	0	1	1
0	1	1	1
1	1	1	1
1	0	1	1

A and B C drop out and C and D are not inverted.

$C \cdot D$
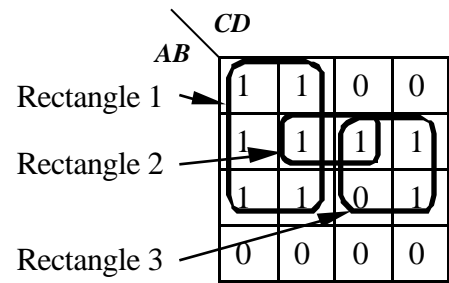
The final answer is:

$\overline{A} \cdot \overline{B} \cdot \overline{D} + A \cdot D + C \cdot D$

6. For the Karnaugh map to the right, identify the problems with each of the three rectangles shown. (2 points each)

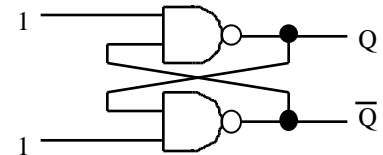Rectangle 1: Total number of cells is NOT a power of 2

Rectangle 2: Completely duplicated by rectangles 1 and 2. It is unnecessary.
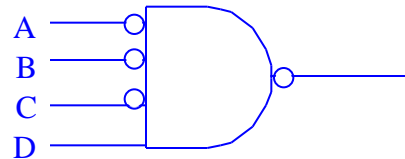
Rectangle 3: Contains a zero.

CD

AB

Rectangle 1

Rectangle 2

Rectangle 3

1	1	0	0
1	1	1	1
1	1	0	1
0	0	0	0

7. For the circuit to the right, what value does Q have? (2 points)

a.) 0   c.) Must know previous value for Q to answer.
b.) 1   d.) Illegal state. Should never have these inputs.
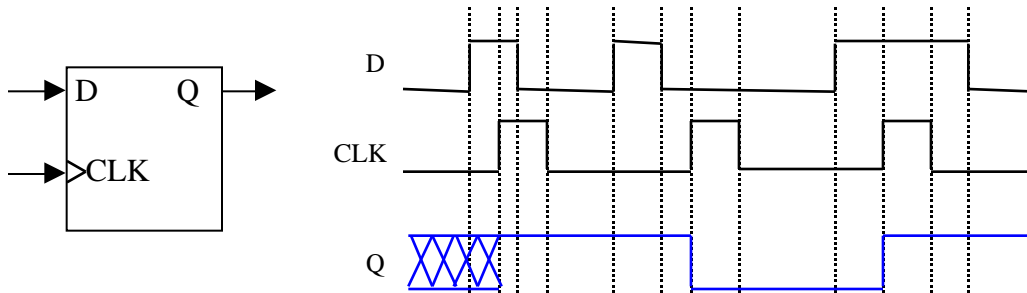
The SR flip-flop truth table indicates that when both inputs equal 1, the previous value of Q and ^Q are maintained. Therefore, the answer is C. (The only illegal state is when both inputs equal 0.)
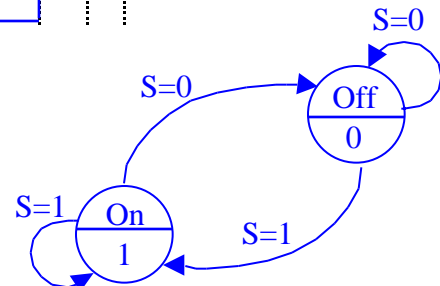
8. In the space to the right, draw the **decoding logic circuit** with an **active-low output** for the inputs A = 0, B = 0, C = 0, and D = 1. (5 points)

A
B
C
D

9. Show the D flip-flop output waveform Q based on the inputs D and CLK indicated in the figure below. Assume the flip-flop captures on the rising edge. (6 points)
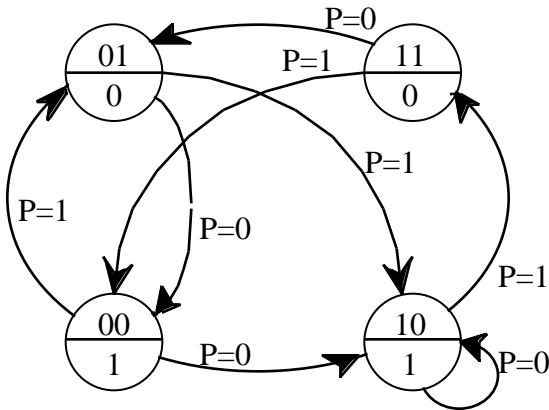
D   Q

>CLK

D

CLK

Q

10. The states to the right define the two states of a light bulb. Assume that you have a switch defined as an input S. S=0 should turn the light off and S=1 should turn the light on. Complete the state diagram by drawing ALL of the transitions based on the input S. (4 points)

S=0

S=0   Off
         0

S=1   On   S=1
         1

11. How many latches or flip-flops are needed to realize a state machine with 16 states? (3 points)

A state machine with 16 states requires numbers from 0 to 15 to uniquely number each state. (Remember to begin numbering at 0!) Since 15 is the largest number we need to represent, then it's going to require the most digits to be stored by flip-flops. Since $15_{10} = 1111_2$, then 4 digits are needed and therefore, 4 flip-flops are needed.

12. Create the next state truth table and the output truth table for the state diagram below. Use the variable names S_1 and S_0 to represent the most significant and least significant bits respectively of the binary number identifying the state. (8 points)
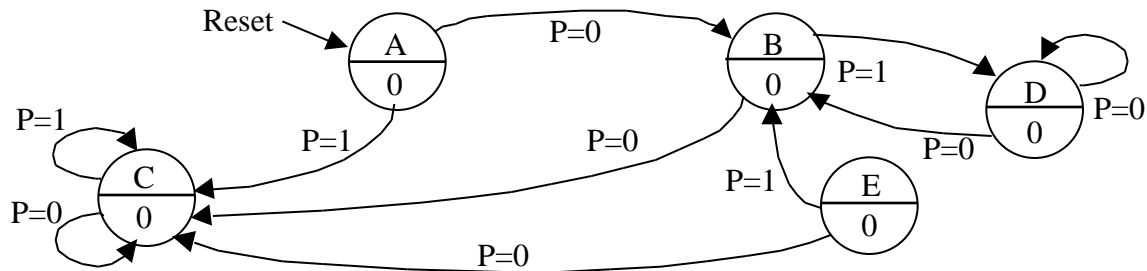

Next State T.T.

S_1	S_0	P	S_1'	S_0'
0	0	0	1	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	0	1
1	1	1	0	0

Output T.T.

S_1	S_0	S_1'
0	0	1
0	1	0
1	0	1
1	1	0

13. Identify the two errors in the above state diagram. Do not bother to correct them. (6 points)

Error 1: There is no way to get to state E. It is extraneous. (Important: There IS a way to get to state A. It is the state that the system goes into when the reset button is pressed or when the system is first powered up.)
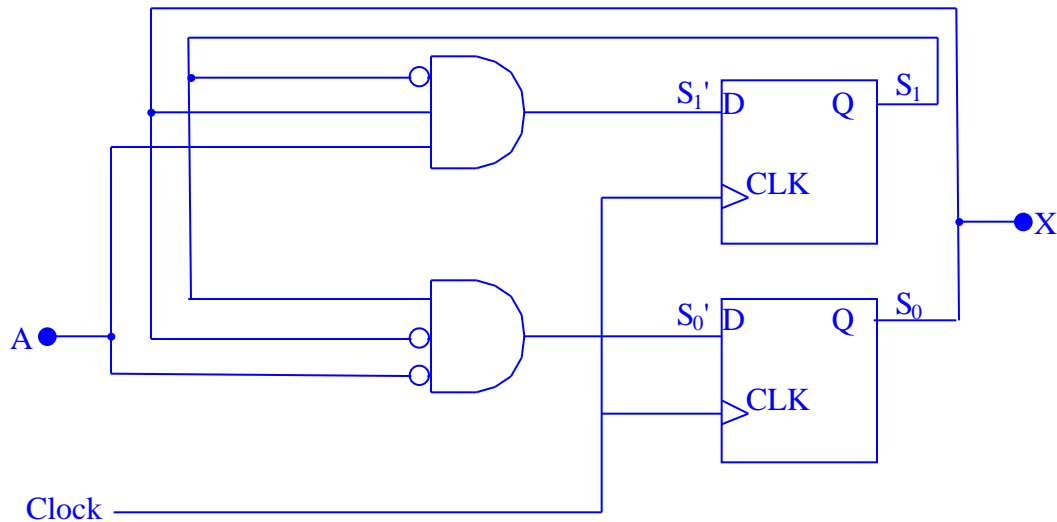Error 2: The transition from state D for P=0 is defined twice while the transition for P=1 is never defined.

14. The three Boolean expressions below represent the **next state bits (S_0' and S_1')** and the **output bit X** based on the **current state (S_0 and S_1)** and the **input A**. Draw the logic circuit for the state machine including the flip-flops and output circuitry. Be sure to label flip-flop inputs and other signals. (8 points)
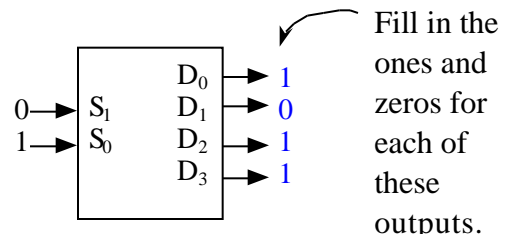
$$S_0' = \overline{S_0}S_1\overline{A} \qquad\qquad S_1' = S_0\overline{S_1}A \qquad\qquad X = S_0$$

15. For the **active-low** output decoder shown to the right, fill in the values for all of the outputs D_0 through D_3. Assume S_1 is most significant bit. (3 points)

Fill in the ones and zeros for each of these outputs.

16. When data is passed from the processor to a memory chip, what values do the bus signals $\overline{R}$ and $\overline{W}$ have? (2 points)
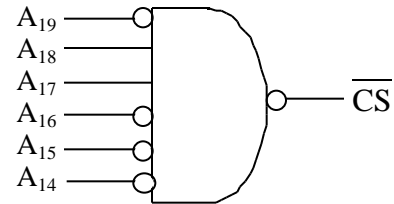
a.) $\overline{R} = 0, \overline{W} = 0$ b.) $\overline{R} = 0, \overline{W} = 1$ c.) $\overline{R} = 1, \overline{W} = 0$ d.) $\overline{R} = 1, \overline{W} = 1$

When data is passed to from the processor to a memory chip, the processor is "writing". Therefore, the active low signal ^W is pulled to zero to indicate this operation and ^R is left to one to indicate it is idle. Therefore, the answer is C.

17. For the active low chip selects ^CS1, ^CS2, and ^CS3, what values will they have if the processor is communicating with the memory chip connected to ^CS3? (3 points)

$\overline{CS1} = \underline{\quad 1 \quad}$ $\overline{CS2} = \underline{\quad 1 \quad}$ $\overline{CS3} = \underline{\quad 0 \quad}$

18. What are the high and low addresses (in hexadecimal) of the memory range defined with the chip select shown to the right? (6 points)

There are 20 address line. This is found by noting that the highest address line has a subscript of 19 and therefore, since we begin counting at 0, we know that there are 20 address lines. Looking at the inputs to the NAND gate, we see that to set ^CS to zero, their values must be: $A_{19}=0$, $A_{18}=1$, $A_{17}=1$, $A_{16}=0$, $A_{15}=0$, and $A_{14}=0$. Therefore, the address lines have the following values for the high and low address:

```
Low address:   0110 0000 0000 0000 0000₂ = 60000₁₆
High address:  0110 0011 1111 1111 1111₂ = 63FFF₁₆
```

19. For the chip select in problem 18, how big is the memory space for this processor? (3 points)

The memory space is determined by the total number of address lines, in this case 20. Therefore, the memory space equals:

$$2^{20} = 1 \text{ Meg}$$

20. For the chip select in problem 18, how big is the memory chip that uses this chip select? (3 points)

The size of the memory chip is determined by the number of bits left undefined by the chip select. In other words, the number of addresses available in the memory chip is equal to the number of combinations of 1's and 0's for the address lines remaining after defining the chip select. Since address lines A_0 through A_{13} are left undefined (14 lines), then the memory chip size equals:

$$2^{14} = 2^{(4+10)} = 2^4 * 2^{10} = 16 * 1\text{K} = 16\text{K}$$

21. True or false: A single memory space can have a low address of $A600_{16}$ and a high address of $AFFF_{16}$. (2 points)

A valid memory space can draw a vertical line separating the chip select inputs from the memory chip's address lines where all the bits to the left for both the high and low addresses stay the same and all the bits to the right are zeros for the low address and ones for the high address. Note that we cannot do this. Neither of the following works.

```
A600₁₆ =  1010 0110 0000 0000₂
AFFF₁₆ =  1010 1111 1111 1111₂
```

```
A600₁₆  =  1010 0110 0000 0000₂
AFFF₁₆  =  1010 1111 1111 1111₂
```

Therefore, the answer is FALSE.

22. True or false: A 1K memory chip can have a low address of $5C00_{16}$. (2 points)

A 1K memory chip uses 10 address lines. Therefore, the low address must have zeros for ALL of its lowest 10 bits. Since the lowest 10 bits of $5C00_{16}$ are zeros, then the answer is TRUE.

```
5C00₁₆  = 0101 1100 0000 0000₂
```

23. True or false: The same chip select should work regardless of the number of data lines connecting the processor to the memory chip. (2 points)

TRUE: The width of the data bus, i.e., the number of bits stored at each address, has no effect on the chip select or other features involving the address.

24. Using logic gates, design a chip select for a 2K RAM placed in a 64K memory space with a low address of 3800_{16}. **Label all address lines used for chip select.** (7 points)

$64K = 64 * 1K = 2^6 * 2^{10} = 2^{(6 + 10)} = 2^{16}$
Therefore, the processor has 16 address lines coming out of it. (A_0 through A_{15})

$2K = 2 * 1K = 2^1 * 2^{10} = 2^{(1 + 10)} = 2^{11}$
Therefore, the memory chip has 11 address lines going into it. (A_0 through A_{10})

Therefore, the chip select using the top $16-11 = 5$ address lines. (A_{11} through A_{15})

Now, convert 3800_{16} to binary to find the binary values for A_{11} through A_{15}.

$3800_{16} =$ 0011 1000 0000 0000₂

$A_{15} = 0$, $A_{14} = 0$, $A_{13} = 1$, $A_{12} = 1$, and $A_{11} = 1$. Therefore, the NAND circuit for the chip select is: