CS/EE 5710/6710 — Digital VLSI Design

Midterm

Tuesday, November 11th, 2003

Name:

Instructions This is a closed-book, closed-notes exam. I want to see what you've learned by coming to lectures, reading, and working on your project, not what you can look up in the textbook. The subjects of the questions are things that I think you should know having been involved in the class to this point.

Work independently. Show your work! Answers with no justification will not be given credit. *Don't Panic!*

Put your name at the top of each sheet of the exam before you start!

1	10 points	
2	24 points	
3	18 points	
4	18 points	
5	15 points	
6	15 points	
Total	100 points	

1 Multiple Choice Questions: 10 points

Choose the one best answer:

a. Which of the following is true for an nmos transistor operating in its *linear* or *triode* mode? (Vgs = gate to source voltage, Vds = drain to source voltage, Vt = threshold voltage)

   (a) Vds < (Vgs - Vt)
   (b) Vds > (Vgs - Vt)
   (c) Vgs < Vt
   (d) Vgs = 0v

b. Which is the best description of the "body effect?"

   (a) Rise in transistor threshold due to increased source to substrate (body) voltage
   (b) Current leaking out the body (substrate) terminal of the transistor due to thin gate oxides
   (c) Mobility variation due to the type of charge carrier in the transistor substrate (body)
   (d) Substrate (body) current caused by impact ionization of hot electrons at the drain

c. The capacitance of a transistor gate is proportional to what?

   (a) The width of the gate
   (b) The length of the gate
   (c) The area of the gate
   (d) The depth of the channel

d. The *hold time* of a sequential device (like a flip flop) is defined to:

   (a) Ensure that the next stage is ready to receive data.
   (b) Ensure that the data are not removed too soon after the clock is applied
   (c) Ensure that the input data have settled before the clock is applied.
   (d) Ensure that the outputs change at the proper time.

e. Which of the following processing techniques would be used to create the source and drain regions of a transistor?

   (a) Oxidation
   (b) Ion implantation
   (c) Sputtering
   (d) Polysilicon deposition

2 Short Answer Questions: 24 Points

Please answer the questions concisely. I'm not looking for a dissertation on each subject, just a brief description of the important ideas.

2.1 Circuit Characterization: 6 points

Why do we measure the propagation delay of a combinational logic gate from 30% of the input voltage swing to 70% of the output voltage swing? What might happen if we used 50% to 50% measurements?

2.2 Circuit Characterization: 6 points

What is meant by "rise resistance" in a characterization of a cell for synopsys? How does it relate to cell timing?

2.3 Logical Effort: 6 points

How would you go about using Logical Effort to design a circuit that starts with a unit-sized inverter (1.5u nmos and 3u pmos) and that eventually has to drive a load 100 times as large as the unit inverter's input load? You don't need to solve the equations, just describe the design process and the important concepts.

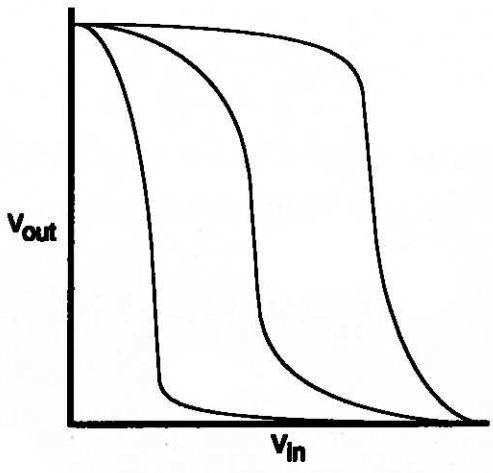
2.4 Transistor Sizing: 6 points

You can bias the switching point of an inverter by changing the relative strength of the PMOS and NMOS transistors in the inverter. The following graph shows the output voltages of three inverters with different switching points due to different transistor size ratios. Label each of the three curves on the graph to indicate which one corresponds to:

A : $\beta_n/\beta_p = 1$

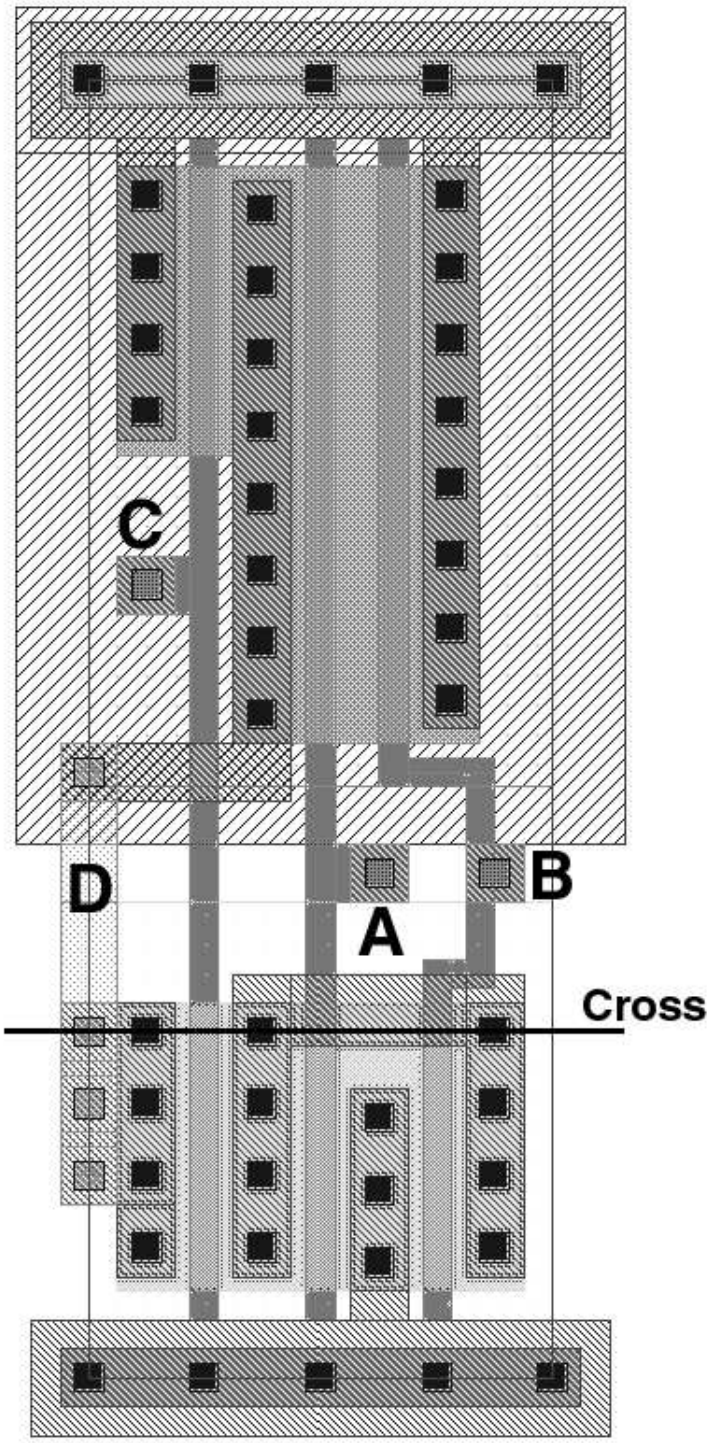
B : $\beta_n/\beta_p = 0.1$

C : $\beta_n/\beta_p = 10$



3 Layout Extraction: 18 points

What function is performed by the following CMOS layout? Extract and draw the transistor schematic of the circuit and define the funcion. (Ignore the “Cross” line for now...)



4 Processing: 18 points

Now consider the "Cross" line. From the layout on the previous page, draw a cross section of the fabricated circuit through the line marked "Cross." That is, slice the chip on that line and show the structure (looking at the sliced edge) that was fabricated to build that circuit. Label each layer in your cross section. Assume an N-well CMOS process like the one we've been talking about in class.

5 Circuit Design: 15 points

Design a single complex static CMOS gate (i.e. one pullup network and oue pulldown network, not a tree of pre-designed gates) that implements the following function. You can assume that inverted versions of the input literals are available (i.e. you don't have to draw the inverters for inverted inputs). In particular:

a. Draw a minimized transistor level schematic for the complex gate (use the fewest possible transistors)

b. Draw an Euler diagram and use it to choose a variable ordering for a line-of-diffusion style layout

c. Draw a stick diagram of a layout using that variable ordering

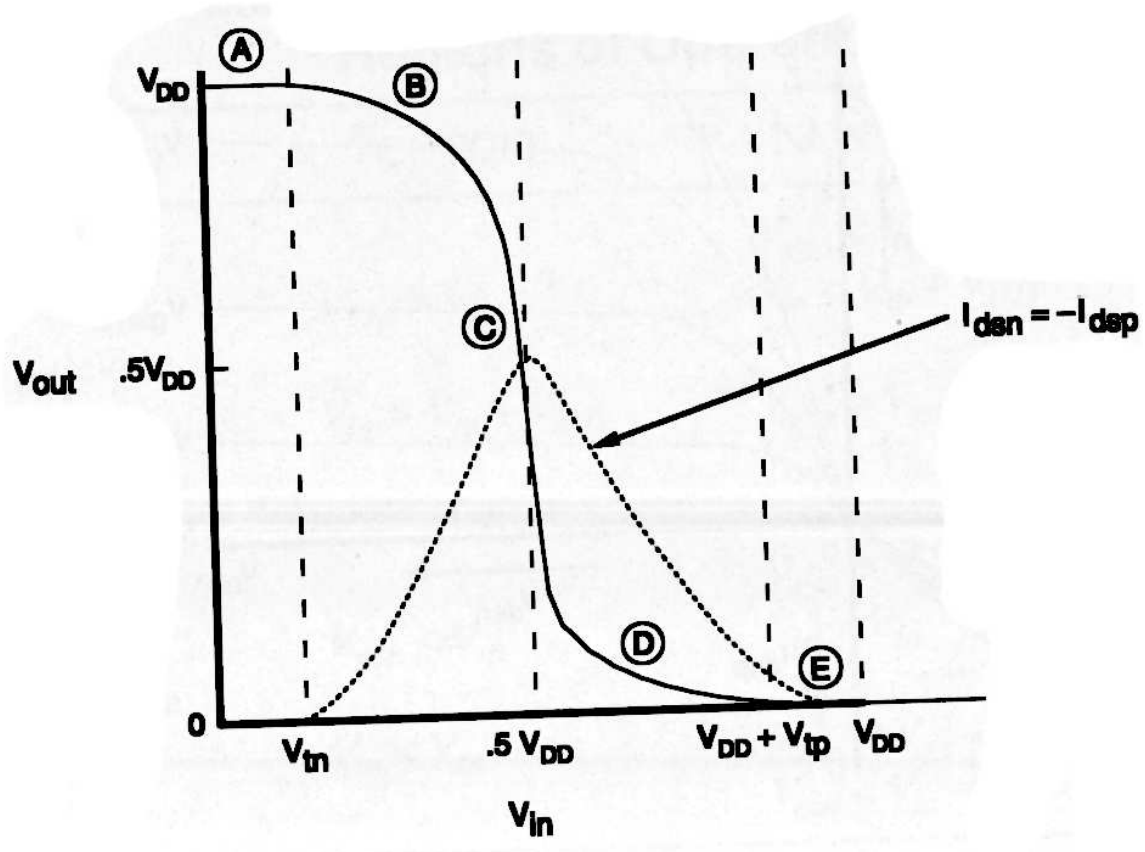
$$F = A\,C\,D\; + A\,B\,\overline{D}$$

6 Inverter Operation: 15 points

6.1 Transistor Operating Regions: 10 points

Given the following diagram of the transfer function of a **CMOS inverter**, fill in the following table for each defined region in the graph. For each region determine if each of the transistors is in its *cutoff*, *linear*, or *saturated* mode. (Hint, look at the first multiple choice question to remind yourself of the voltages that define each of the three regions of operation.)(Ignore the dotted Ids line for now.)

Region	Transistor	Mode of operation
A	PMOS NMOS	
B	PMOS NMOS	
C	PMOS NMOS	
D	PMOS NMOS	
E	PMOS NMOS	



6.2 Inverter Power: 5 points

In the figure on the previous page, the Ids (drain to source current) curve is shown as the dashed line. Explain why that curve is shaped the way it is. What does this curve shape imply about power consumption of an inverter?