CS/EE 6710 -- CAD Assignment #1

Due Friday, September1st, 5:00pm
Put assignments in the slot outside the SoC office

For this assignment you'll use *Crafting a Chip: A Practical Guide to the UofU CAD Flow*. You'll need to look at Chapters 1-4 for this assignment. The chapters are tutorial in nature so you should be able to follow along as you're trying out the tools. I recommend that you don't print them out. They're somewhat long in the first place because of the step-by-step nature of the tutorials, and they're likely to change over the course of the semester as they are refined.

1. Complete the first part of the Cadence Composer tutorial in Chapter 3 by designing a Full Adder using the standard cells in the **NCSU_Digital_Parts library**. Create a symbol for the Full Adder and use it in building a 3-bit Adder. Simulate the 3-bit Adder using VerilogXL or NC_Verilog and observe the timing diagrams.
2. Complete the next part of the tutorial in Chapter 3 by designing a 2-input NAND gate using **nmos** and **pmos** transistors from the **UofU_Analog_Parts library**. Create a symbol for the NAND. Put your new NAND gate into another schematic for testing (which will include input and output pins, etc). Simulate it using VerilogXL or NC_Verilog and observe the timing diagrams.
3. Using instances of the 2 input NAND gate that you have created, build a circuit that implements the following Boolean function (don't minimize or manipulate the function, and don't use any gates except for your own NAND gate):

$$F = \overline{A}\,\overline{B} + AC + B\overline{C}$$

4. Simulate it using Verilog XL or NC_Verilog and observe the timing diagrams. (This part you have to do on your own.)

For all three of these tasks, make sure that your Verilog test fixture uses "if" and "$display" statements to check for the correct results in the simulation. You should be able to tell from running your test fixture whether the circuit is working correctly before you look at the timing waveforms (that is, if the circuit produces an incorrect output, an error message should be printed!). Also, make sure to use an **Asheet** frame on every schematic! Spend the time to make your schematics neat and orderly! Straighten out the wires, space out the components appropriately, don't over crowd, and generally make things look nice.

Note that this assignment is to be done individually! We'll form teams later.

Things to Turn In

Turn in hardcopies of:

1. Gate-level schematics of the Full Adder, 3-bit Adder, their Verilog test fixtures, simulation logs and timing diagrams
2. Transistor-level schematic of the 2 input NAND gate, Verilog test fixtures, simulation logs and timing diagrams
3. Schematic of the Boolean function using your new NAND gate, the Verilog test fixtures, simulation logs and timing diagrams

Information about the schematic capture tool, Verilog simulation, printing the simulation logs, etc. can all be found in the CAD Manual.

Make sure your name is easily visible on all the pages you turn in. Turn in assignments to the box outside the SoC (School of Computing) front office.