CS/EE 6710 -- CAD Assignment #2

Due Thursday, September 14th, 5:00pm
Put assignments in the slot outside the SoC office

1. Design an inverter using transistors in a Composer schematic and simulate the inverter both with Verilog, and with Analog Environment with Spectre. (This is covered in Chapters 3, 4, and 6 in the lab manual)
2. Draw the layout for the inverter in Virtuoso, extract and simulate this inverter with Spectre. Run DRC and LVS. Compare the waveforms. (This is covered in Chapter 5 of the lab manual)
3. Draw a layout for the two-input NAND gate that you designed in CAD assignment #1. Simulate that layout using Spectre and compare against the Verilog simulation from CAD #1. Verify the NAND gate layout with DRC and LVS against the transistor version from CAD #1.
4. Use the layout of the NAND gate and inverter to design the layout of the function from Cad #1 in Virtuoso. Modify the schematic for the function to use the inverter and NAND instead of only NAND gates. Remember that the function you're implementing is:

   $$F = \overline{A}\,\overline{B} + AC + B\overline{C}$$

   In the layout you should include instances of the layout for the NAND and layout for the inverter in a new layout view, make the connections by drawing layout to connect them. Simulate this layout in Spectre. Verify with DRC and LVS against the modified schematic.

Turn in hardcopies of:

1. All schematics, layouts, Verilog simulation tesetbenches and results Spectre simulations (waveforms), and LVS logs.

Note about LVS logs: You don't need to print out the DRC logs. You should note that if it doesn't pass the DRC step, it won't pass the LVS step. So you just need to hand in the LVS logs. You can get to the LVS log in two ways.

1. In the LVS window after you finish the LVS step, you need to press the output button to view the LVS log. In the LVS log window, do a File ->save as and save

it to a file. Now you can print this file.

2. Otherwise, in your ~/IC_CAD/cadence/LVS directory, you will find a file called 'si.out'. This is your LVS log file. This is the same file as in the previous step.