Points missed: _____ Student's Name: _____

Total score: _____/100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 3 for Spring Semester, 2005

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes.
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- ***Calculators are not allowed.*** Use the tables below for any conversions you may need. Leaving an answer as a numeric expression is acceptable.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

1. How many latches (memory cells holding one bit of data) does an SRAM with 24 address lines and 16 data lines have? Leave your answer in the form of an equation with numeric values. (2 points)

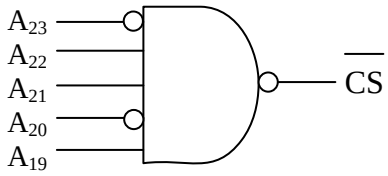
2. Circle ***all*** that apply. A storage cell in an SRAM: (4 points)

   a.) is volatile b.) is a capacitor c.) is cheaper than cells in a DRAM
   d.) is a latch e.) must be refreshed regularly f.) is smaller than cells in a DRAM
   g.) is typically used for main memory h.) is faster than an DRAM

3. Match each of the settings of the bus control signals $\overline{R}$ and $\overline{W}$ on the left with the bus operation on the right. (3 points)

$\overline{R}$	$\overline{W}$			Operation of the bus
0	0	☐	☐	Illegal setting
0	1	☐	☐	The bus is idle
1	0	☐	☐	Processor reads from memory
1	1	☐	☐	Processor writes to memory

4. What are the high and low addresses (in hexadecimal) of the memory range defined with the chip select shown to the right? (6 points)



Low address: _____ High address: _____

5. For the chip select in problem 4, how big is the memory chip that uses this chip select? (3 points)

6. For the chip select in problem 4, how big is the memory space of the processor whose address lines are used for the chip select? (3 points)

7. True or false: The address range 65000_{16} to $66FFF_{16}$ is a valid range for a single memory. (2 points)

8. What is the largest memory that can have a starting (lowest) address of $8C000_{16}$? (3 points)

9. Using logic gates, design an active low chip select for a RAM placed in a 1 Meg memory space with a low address of 30000_{16} and a high address of $37FFF_{16}$. ***Label all address lines used for chip select.*** (6 points)

10. True or false: The rotational speed of the platter(s) measured in rotations per minute (RPM) of a ***multiple zone recording*** hard drive varies depending on the position of the head. (2 points)
11. True or false: A small gap is left between the ends of adjacent sectors on a single track of a hard drive disk in order to avoid data bleeding over from one sector to the other. (2 points)
12. True or false: When storing data to the magnetic material coating the surface of a hard drive platter, one direction of magnetic polarization represents the logic ones while the other direction represents the logic zeros. (2 points)
13. Describe how the LRU replacement algorithm for the fully associative mapping algorithm works. (3 points)

The table below represents a small section of a cache that uses fully associative mapping. Refer to it to answer questions 14, 15, 16, and 17. Assume the processor's memory bus uses 20 bits for an address.

Tag (binary values)	Word within the block							
	000	001	010	011	100	101	110	111
01001001101010010	00_{16}	61_{16}	$C2_{16}$	23_{16}	84_{16}	$E5_{16}$	46_{16}	$A7_{16}$
11001100101110100	10_{16}	71_{16}	$D2_{16}$	33_{16}	94_{16}	$F5_{16}$	$\mathbf{56_{16}}$	$B7_{16}$
00011101100110101	20_{16}	81_{16}	$E2_{16}$	43_{16}	$A4_{16}$	05_{16}	66_{16}	$C7_{16}$
10110011110011010	30_{16}	91_{16}	$F2_{16}$	53_{16}	$B4_{16}$	15_{16}	76_{16}	$D7_{16}$
01011001111001101	40_{16}	$A1_{16}$	02_{16}	63_{16}	$C4_{16}$	25_{16}	86_{16}	$E7_{16}$
01001010110010010	50_{16}	$B1_{16}$	12_{16}	73_{16}	$D4_{16}$	35_{16}	96_{16}	$F7_{16}$
	col 0	col 1	col 2	col 3	col 4	col 5	col 6	col 7

14. From what address in main memory did the value 56_{16} (the value in bold) come from? Leave your answer in binary. (3 points)

15. A copy of the data from memory address $59E6E_{16}$ is contained in the portion of the cache shown above. What is the value stored at that address? (3 points)

16. If the block containing memory address $A46FD_{16}$ were to be loaded into the cache described above, what would the tag be? (2 points)

17. What column (0 through 7) would the data item from the previous problem be stored in? (2 points)

18. Assume a processor takes 3 cycles to execute any instruction (fetch, decode, execute)
    a. How many cycles would a ***pipelined*** processor take to execute 8 instructions? (2 points)

    b. How many cycles would a ***non-pipelined*** processor take to execute 8 instructions? (2 points)

19. If a processor compares two values, what are the settings of the zero flag and sign flag if the two values are equal? (2 points)

    ZF = _____ SF = _____

20. Which 80x86 pointer/index register points to the function parameters stored in the stack? (2 points)

21. Which two 80x86 pointer/index registers are used for string functions. (3 points)

22. Name the two benefits of the segment/pointer addressing system of the 80x86. (3 points)

Answer questions 23 through 26 using the following settings of some of the 80x86 registers.

```
AX = 1234h      SP = 3021h      CS = 1000h
BX = 4321h      SI = 4356h      SS = 2000h
CX = 0101h      DI = 1423h      DS = 3000h
DX = FEDCh      BP = 5987h      ES = 4000h
```

23. What is the value contained in the register DH? (2 points)

24. What is the physical address pointed to by ES:DI? (3 points)

25. True or false: The physical address of the next instruction to be executed by the processor can be calculated from the above data? (2 points)

26. True or false: The physical address of the last item to be stored to the stack can be calculated from the above data? (2 points)

27. Assume AX=1000h, BX=2000h, and CX=3000h. After the following code is executed, what would AX, BX, and CX contain? (3 points)

```
PUSH CX
PUSH BX
PUSH AX
POP BX
POP CX
POP AX
```

Place your answers in space below:

AX =

BX =

CX =

28. Using an original value of 00111100_2 and a mask of 00001111_2, calculate the results of a bitwise AND, a bitwise OR, and a bitwise XOR for these values. (2 points each)

Original value	Bitwise operation	Mask	Result
00111100_2	AND	00001111_2	
00111100_2	OR	00001111_2	
00111100_2	XOR	00001111_2	

29. For each of the following binary bit patterns, set the parity bit for odd parity, i.e., the same parity settings as used by the 80x86 processor parity flag.

Binary value	Parity	
1 0 1 0 1 0 1 1	_____	(1 point)
1 0 1 1 0 1 1 1	_____	(1 point)
1 0 0 1 1 1 0 1	_____	(1 point)

30. If the datasum calculated from a sequence of values is a decimal 95, what would the decimal value of the 2's complement checksum be? (2 points)

31. Describe the primary drawback discussed in class of parity checks. (2 points)

32. Describe one of the two reasons discussed in class for using an XOR "borrow-less" subtraction in the calculation of a CRC. (2 points)

33. True or false: The order of operands in an XOR "borrow-less" subtraction does not matter, e.g., A – B = B – A in a borrow-less subtraction. (2 points)

34. Circle ***all*** of the following statements that are true for the use of a CRC as a method of data verification in serial communications. (6 points)

    a. They out perform basic checksums by translating minor changes in the data into significant changes in the check value.
    b. The number of bits in the divisor must be exactly one bit longer than the number of bits per data item being transmitted.
    c. A zero result from performing a CRC on received data indicates that the data was error free.
    d. Both the transmitting device and the receiving device must use the same polynomial (divisor) for calculation of the CRC.
    e. The transmitting device must wait until it is finished computing the CRC before sending any of the serial data stream.
    f. The quotient resulting from the long-division used to calculate the CRC is of no importance to the verification of the data. Only the remainder is used.