Points missed: _____ Student's Name: _____

Total score: _____/100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 3 for Spring Semester, 2003

Section 002

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes.
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- ***Calculators are not allowed.*** Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

DEC - Decrement
Usage: DEC dest
Modifies flags: AF OF PF SF ZF
Description: Unsigned binary subtraction of one from the destination.

INC - Increment
Usage: INC dest
Modifies flags: CF AF OF PF SF ZF
Description: Adds one to destination unsigned binary operand.

Jxx - Jump Instructions Table

Mnemonic	Meaning	Jump Condition
JE	Jump if Equal	ZF=1
JG	Jump if Greater (signed)	ZF=0 and SF=OF
JGE	Jump if Greater or Equal (signed)	SF=OF
JL	Jump if Less (signed)	SF != OF
JLE	Jump if Less or Equal (signed)	ZF=1 or SF != OF
JMP	Unconditional Jump	unconditional
JNB	Jump if Not Below	CF=0
JNE	Jump if Not Equal	ZF=0
JNG	Jump if Not Greater (signed)	ZF=1 or SF != OF
JNL	Jump if Not Less (signed)	SF=OF
JZ	Jump if Zero	ZF=1

MOV - Move Byte or Word
Usage: MOV dest,src
Modifies flags: None
Description: Copies byte or word from the "src" operand to the "dest" operand.

NOT - One's Compliment Negation (Logical NOT)
Usage: NOT dest
Modifies flags: None
Description: Inverts the bits of the "dest" operand forming the 1s complement.

POP - Pop Word off Stack
Usage: POP dest
Modifies flags: None
Description: Transfers word at the current stack top (SS:SP) to the destination then increments SP by two to point to the new stack top. CS is not a valid destination.

PUSH - Push Word onto Stack
Usage: PUSH src
Modifies flags: None
Description: Decrements SP by the size of the operand (two or four, byte values are sign extended) and transfers one word from source to the stack top (SS:SP).

SAL/SHL - Shift Arithmetic Left / Shift Logical Left
Usage: SAL dest,count SHL dest,count
Modifies flags: CF OF PF SF ZF (AF undefined)
Shifts the destination left by "count" bits with zeroes shifted in on right. The Carry Flag contains the last bit shifted out.

SAR - Shift Arithmetic Right
Usage: SAR dest,count
Modifies flags: CF OF PF SF ZF (AF undefined)
Shifts the destination right by "count" bits with the current sign bit replicated in the leftmost bit. The Carry Flag contains the last bit shifted out.

1. For each of the following registers, identify how many bits they contain. (4 points)

   AH = _____ bits ES = _____ bits BP = _____ bits SI = _____ bits

   Answer:
   AH has 8 bits
   ES (extra segment) is a segment register and it has 16 bits
   BP (base pointer) is a pointer register and it has 16 bits
   SI (source index) is a pointer register and it has 16 bits

2. Each of the following registers is typically paired with a second register to be used with segmented addressing. Identify the name of the register it is usually paired with and describe the purpose of the pair, i.e., what function do they serve when used together for segmented addressing? (8 points)

Register Pair	Purpose
CS: _IP__	The code segment:instruction pointer points to the next instruction for the processor to execute.
_DS_: SI	The data segment:source index is used to point to data to be retrieved from memory.
_DS_: DI	The data segment:destination index is used to point to a memory location to store data to.
SS: _SP_	The stack segment:stack pointer points to the top of the stack which can be used as temporary storage of register values

3. List the two benefits of segmented addressing. (4 points)

   1. Relocate-able code
   2. Allows the 8086 processor to address a 20 bit address space with only 16 bit registers

Answer questions 4 through 9 based on the following settings of register values in an 8086

AX =	10FFh	SP =	0012h	CS =	F000h
BX =	8745h	BP =	1032h	DS =	E000h
CX =	ABCDh	DI =	2052h	SS =	D000h
DX =	1111h	SI =	3072h	ES =	C000h

4. What value does CH contain?

   AB_{16} (2 points)

5. What value does BL contain?

   45_{16} (2 points)

6. Assume that the instruction **`INC AL`** is executed. How would the following flags be set? Write "N/A" if the flag was not affected. (3 points)

   ZF = _____ CF = _____ SF = _____

   Looking at the list of instructions on the previous page, we see that the INC command increments the operand by one and affects CF, AF, OF, PF, SF, and ZF, i.e., all of the flags we list above. Since AL equals FF_{16}, adding one should result in a carry propagating through the register with the final result of 00_{16} and a 1 in the carry. Therefore, since the result is zero, ZF=1. The most significant bit is 0 which makes SF=0. The operation resulted in a carry, and therefore CF=1.

7. Assume that the instruction **`MOV CX,0000h`** is executed. How would the following flags be set? Write "N/A" if the flag was not affected. (3 points)

ZF = _____ CF = _____ SF = _____

Looking at the list of instructions, we see that the MOV command moves the second operand into the first operand. In addition, (and most importantly) none of the flags are affected. Therefore, the answer is:

ZF = _N/A___ CF = _N/A___ SF = _N/A___

8. What is the physical address pointed to by the segment:pointer pair ES:BP? (3 points)

ES:BP → C000h:1032h. Add a zero to the end of the segment register's value, then add the pointer register's value.

```
 C0000
+ 1032
-------
 C1032
```

The physical address is therefore $C1032_{16}$.

9. True or False: From the information above, the physical address of the top of the stack can be calculated, e.g., the address from which data would be retrieved for a POP instruction. (2 points)

Since the physical address of the stack is derived from the stack segment (SS) and the stack pointer (SP) and since both of those are available from the table above, the answer is true.

10. Of the following jump instructions, indicate which ones will jump to the address LOOP, which ones will simply execute the next address (i.e., not jump), and which ones you don't have enough information to tell.

Instruction		Current Flags	Jump to LOOP	Not jump to LOOP	Cannot be determined	
JL	LOOP	SF=1, ZF=0	❑	❑	☒	(2 points)
JE	LOOP	SF=0, ZF=1, CF=0	☒	❑	❑	(2 points)
JNE	LOOP	SF=0, ZF=1, OF=1	❑	☒	❑	(2 points)

11. Using an original value of 10011010_2 and a mask of 00001111_2, calculate the results of a bitwise AND, a bitwise OR, and a bitwise XOR for these values. (2 points each)

Original value	Bitwise operation	Mask	Result
10011010_2	AND	00001111_2	00001010_2
10011010_2	OR	00001111_2	10011111_2
10011010_2	XOR	00001111_2	10010101_2

12. For each of the assembly language commands below, identify what the first and second operands are referring to, a constant (C), a register (R), or memory location (M). (The first operand is the one to the left of the comma). (7 points)

```
je    1234h
mov   [ax],1999h
adc   bh,[ax]
sar   bx,4
```

1st operand	2nd operand
C	
M	**C**
R	**M**
R	**C**

13. Assume AX=1234h, BX=FEDCh, and CX=0000h. After the following code is executed, what would AX, BX, and CX contain? (3 points)

```
PUSH AX
PUSH BX
PUSH CX
POP AX
POP BX
POP CX
```

Place your answers in space below:

AX = 0000h

BX = FEDCh

CX = 1234h

14. If a processor takes 3 cycles to execute any instruction (fetch, decode, execute), how many cycles would a non-pipelined processor take to execute 8 instructions? (3 points)

A non-pipelined processor simply executes the instructions one at a time with no overlap. Therefore, the number of cycles equals 3 times the number of instructions:

number of cycles = 3 x 8 = 24

15. If a processor takes 3 cycles to execute any instruction (fetch, decode, execute), how many cycles would a pipelined processor take to execute 8 instructions? (3 points)

A pipelined processor overlaps 2 cycles for each instruction. Therefore, it will take 2 cycles to fill the pipeline, then one cycle per instruction to execute each one.

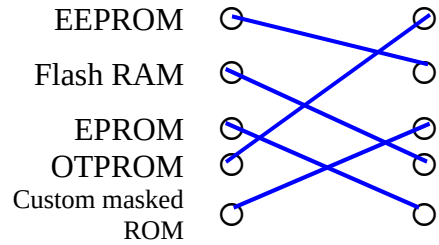
number of cycles = 2 + 8 = 10

16. True or False: DRAM is faster than SRAM. (2 points) **FALSE**

17. True or False: DRAM is cheaper per bit than SRAM. (2 points) **TRUE**

18. True or False: More DRAM can be packed into the same area (higher density) than SRAM. (2 points) **TRUE**

19. Draw a line between the memory type on the left and its most appropriate characteristic on the right. (2 points each)



EEPROM — can be written to by the processor, but has a very slow write time as compared to RAM

Flash RAM — can be used like a miniature solid-state hard drive

EPROM — uses ultraviolet light shined through a small window to erase

OTPROM — best for ***extremely*** large quantities (more than 10,000)

Custom masked ROM — best one for large quantities that can be programmed by user

Questions 20 through 23 are based on the following breakdown of address bits for a direct mapping cache RAM.

9 tag bits	12 line id bits	3 word id bits

20. If each address contains a byte, how many bytes are in a block of memory? (2 points)

$2^3 = 8$ bytes per block

21. If each line in the cache contains a block, how many lines are in the cache? (2 points)

$2^{12} = 4096$ lines in the cache

22. True or False: The block containing the data stored in main memory at address 6B548A would be stored in exactly the same line of the cache as the block containing the data stored in main memory at address B5D48C. (2 points)

To determine which line of the cache a memory address is to be stored in, we must first convert the hex addresses to binary. Then, identify the bits that identify the cache line. (The bits that represent the cache line are shaded in binary below.)

```
6B548A = 011010110101010010001010
B5D48C = 101101011101010010001100
```

Notice that the bit pattern of 1's and 0's is the same for both numbers. Therefore, the two memory addresses are stored in the same location. **TRUE.**

23. Only the first 5 lines of the cache defined above are shown in the table below. Identify the main memory address of the data that is in the shaded cell and contains D8. Note: The tags are given in binary in the table. You may leave your answer in binary if you wish. (3 points)

		Block Data							
Line #	Tag	Word 000	Word 001	Word 010	Word 011	Word 100	Word 101	Word 110	Word 111
0	101101101	11	00	AA	78	90	60	59	48
1	010101101	22	99	BB	56	AB	15	26	37
2	000111000	33	88	CC	34	CD	83	92	01
3	111000111	44	77	D8	12	EF	74	65	56
4	100110101	55	66	EE	FF	10	29	38	47

TAG = 111000111
LINE = 3 = 000000000011
WORD ID = 010

The physical address = 111000111000000000011010

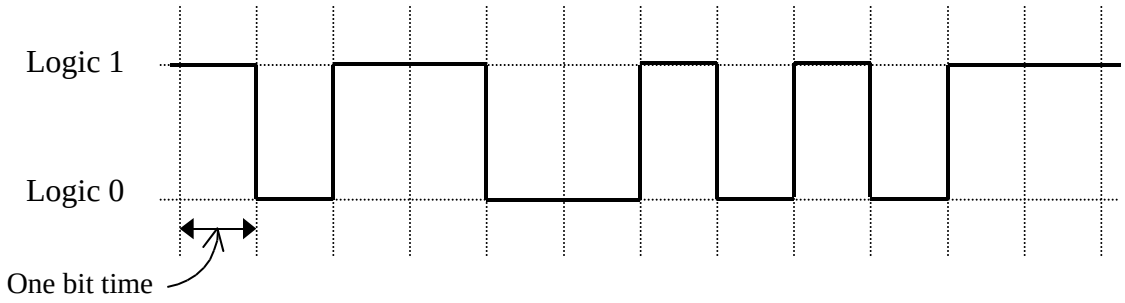
24. In a hard drive containing multiple disks, the group of tracks occurring at the same position on each side of each disk is referred to as a _____. (2 points)

cylinder

25. True or False: Multiple zone recording puts different numbers of sectors on different tracks so that the disk doesn't have to change velocity as the heads move to different tracks. (2 points)

FALSE – Actually, multiple zone recording is set up specifically so that the disk turns at different velocities for different tracks.

Questions 26 through 27 are based on the following RS232 serial signal sent with 8 data bits.



26. What is the binary value being transmitted in this signal? (5 points)

$01010011_2 = 53_{16}$

27. Assuming a parity bit is sent, select the ***two*** possible parity settings from the list below that would make the parity bit valid for this signal. (3 points)

a.) Odd b.) Even c.) Mark d.) Space

The parity bit position (if there is one) is a 1. If we were counting the number of one's, the result would be odd. Therefore, one possible selection would be **ODD PARITY**. If we were simply looking for a set or not set value, then the other selection would be set or **MARK PARITY**.

28. What would an even parity bit be set to for the data 10110110? (2 points)

To make the sum of ones even for even parity, we would need to have a parity bit of 1.

29. What is the maximum number of devices that can be connected to a single RS232 serial connection? (2 points)

2 – RS232 is a point-to-point protocol