

Points missed: \_\_\_\_\_ Student's Name: \_\_\_\_\_

Total score: \_\_\_\_\_ /100 points

East Tennessee State University  
Department of Computer and Information Sciences  
CSCI 4717 – Computer Architecture  
TEST 1 for Fall Semester, 2003  
Section 201

**Read this before starting!**

- The total possible score for this test is 100 points.
- This test is closed book and closed notes
- You may use one sheet of scrap paper that you will turn in with your test.
- **When possible, indicate final answers by drawing a box around them. This is to aid the grader (who might not be me!) Failure to do so might result in no credit for answer.**

**Example:**

**32F1<sub>16</sub>**

- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
$2^4$	16
$2^5$	32
$2^6$	64
$2^7$	128
$2^8$	256
$2^9$	512
$2^{10}$	1K
$2^{20}$	1M
$2^{30}$	1G

“Fine print”

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarizing, the changing or falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

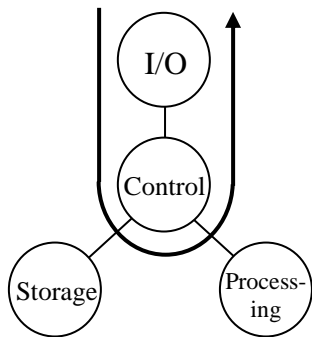
**Short-ish Answer (2 points each)**

1. For each of the following characteristics of system component design, indicate which method of implementation is the best, hardware (HW), software (SW), or firmware (FW), and which is the worst. (1 point for each answer to each characteristic)

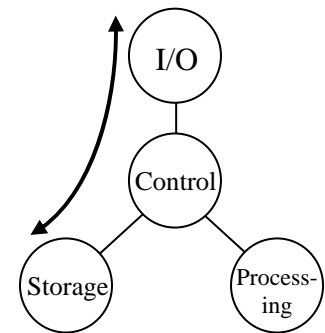
Best	Worst	Characteristic
_____	_____	Keeping development costs down
_____	_____	Keeping manufacturing costs down
_____	_____	High reliability
_____	_____	Making a design that is very flexible or adaptable
_____	_____	Making a high-speed design

2. For the following items, indicate whether the characteristic more closely describes a top-down (TD) or a bottom-up (BU) design method. (2 points each)

- \_\_\_\_\_ Design time is reduced
- \_\_\_\_\_ Typically more expensive
- \_\_\_\_\_ Easier to meet performance goals
- \_\_\_\_\_ Could waste a portion of the available functionality of some components
- \_\_\_\_\_ Developing software for a PC platform relying heavily on software libraries
- \_\_\_\_\_ Past design experience can be drawn upon



3. Give an example of a system where the flow of operation matches that of the figure to the left.



4. Give an example of a system where the flow of operation matches that of the figure to the right.

5. True or False: Although DRAM speed has not kept up with DRAM density, it has successfully kept up with processor speed.

6. Which is the fastest cache mapping function?

- a.) Direct mapping                      b.) Set associative mapping                      c.) Fully associative mapping

*The next 2 questions are based on a system in which a direct access to the cache takes 0.01 uS and a direct access to main memory takes 0.1 uS.*

7. If 80% of the accesses to memory are successfully retrieved from the cache, what is the average memory access time if the cache is connected in parallel to the processor?
  - a.) 0.28 uS    b.) 0.082 uS    c.) 0.008 uS    d.) 0.012 uS    e.) 0.028 uS    f.) None of the above
  
8. How long will an access to *main memory* take if the architecture places the cache between the processor and main memory instead of in parallel with main memory?
  - a.) 0.1 uS    b.) 0.09 uS    c.) 0.12 uS    d.) 0.11 uS    e.) None of the above

*The next 4 questions are based on the small portion shown below of a cache using direct mapping.*

Tag (binary)	Line number (binary)	Word within block				
		00	01	10	11	
0101 0011 01	01 0100 1001 10	0x23	0x56	0xaf	0x3d	Row a
0100 1101 10	01 0100 1001 11	<b>0xff</b>	0xc4	0xa1	0x00	Row b
1010 1101 11	01 0100 1010 00	0x34	0x3a	0x09	0x03	Row c
0110 1011 11	01 0100 1010 01	0x58	0xa5	0x56	0x76	Row d
1011 0101 01	01 0100 1010 10	0x67	0xa2	0xcf	0xf4	Row e
1111 0001 00	01 0100 1010 11	0x9a	0xa3	0xf2	0xf3	Row f
		Col 0	Col 1	Col 2	Col 3	

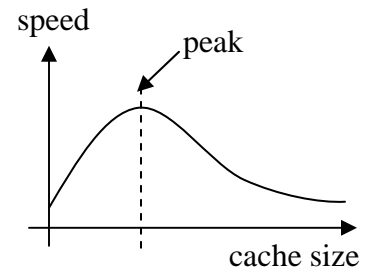
9. A block containing the address 0xB5549B=101101010101010010011011 is not contained in the cache. When loaded, which row (a-f) and column (0-3) will its value be stored in?
  
10. When the block from the previous problem is loaded into memory, what will the tag be?
  
11. What is the main memory address of the data 0xff (row b, column 0) in the section of cache? Leave your answer in binary if you wish.
  
12. The main memory address 0xB554AA = 101101010101010010101010<sub>2</sub> is contained in this cache.
  - a.) True    b.) False    c.) Cannot be determined -- could possibly be elsewhere in the cache
  
13. In a cache using direct mapping with a tag size of 5 bits, a block size of 8 words, and an address length of 16 bits, each block of memory maps to \_\_\_\_\_ line(s) of the cache.
  - a.) only one    c.) one of 8    e.) one of 255    g.) cannot be determined
  - b.) one of 2    d.) one of 32    f.) one of 256    h.) none of the above

14. In a cache using set associative mapping with a tag size of 10 bits, a block size of 8 words, and an address length of 16 bits, each block of memory maps to \_\_\_\_\_ line(s) of the cache.
- a.) only one      c.) one of 8      e.) one of 255      g.) cannot be determined  
 b.) one of 2      d.) one of 32      f.) one of 256      h.) none of the above
15. How many lines does a cache using fully associative mapping have for an address of 10 bits and a block size of 8 words?
- a.) 4 lines      c.) 256 lines      e.) 128 lines      g.) cannot be determined  
 b.) 255 lines      d.) 127 lines      f.) 1024 lines      h.) none of the above
16. True or False: A block from main memory could possibly be stored in *any* line of a cache using fully associative mapping.
17. For single error correction, what is the minimum number of check bits required for 16 data bits?
- a.) 4      b.) 5      c.) 6      d.) 7      e.) 8      f.) 9      g.) 10      h.) 11      i.) 12
18. If it takes a minimum of 8 bits to correct a single error in a 128-bit data word, then how many bits will it take to do single-error correction with double-error detection?
- a.) 8      b.) 9      c.) 10      d.) Cannot be determined      e.) None of the above
19. What is the total number of possible syndrome word values for 8 data bits and 4 check bits if we only allow for the cases of no errors or single bit errors?
- a.) 12      b.) 13      c.) 15      d.) 16      e.) 32      f.) 255      g.) 256      h.) 2047      i.) 2048
20. What is the capacity in terms of the number of *addressable* locations of a DRAM with 14 bits addressing the rows?

***Longer Answers (Points vary per problem)***

21. Name two of the three significant characteristics discussed in class of the Von Neumann architecture. (4 points)

22. The graph to the right represents the average speed of a memory access relative to the size of the cache. Why does the slope decrease to the left (i.e., why does the speed decrease with decreased cache size) before the peak? (3 points)



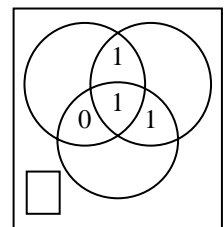
23. Using the graph from the previous question, why does the slope decrease to the right (i.e., why does the speed decrease with increased cache size) after the peak? (3 points)

24. Name three of the five effects discussed in class that Moore's law has had on the contemporary application of computers. (6 points)

25. List an advantage of a split cache. (3 points)

26. Describe the difference between the FIFO and Least Frequently Used cache replacement algorithms. (3 points)

27. Using the graphic to the right, fill in the check code bits AND the extra parity bit that provides double error detection for the 4 bit Hamming Code. The bit for double error detection should be placed in the box in the lower left portion of the figure. (5 points)



28. There are two causes for a DRAM cell to require refreshing. List **both** of them. (4 points)

The following 3 questions use the table below representing the binary position numbers for an 8-bit data word ( $D_7, D_6, D_5, D_4, D_3, D_2, D_1, \text{ and } D_0$ ) with a 4-bit check code ( $C_3, C_2, C_1, \text{ and } C_0$ ). The syndrome word that is derived from the stored code and the code computed when memory is read is all zeros if the no error occurred. Otherwise, if a single bit error occurred, the syndrome word equals the binary position number of the bit that changed.

Binary position number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Bit name	$D_7$	$D_6$	$D_5$	$D_4$	$C_3$	$D_3$	$D_2$	$D_1$	$C_2$	$D_0$	$C_1$	$C_0$

29. If the stored code is 0110 and the code computed when memory is read is 0101, which bit needs to be inverted to repair a single bit error? (2 points)
30. How many bits would need to be added to the check code in order to make this a single-error correction/double error detection code? (2 points)
31. Write the equation to generate check code bit  $C_2$  from the data bits  $D_7$  through  $D_0$ . (3 points)

32. List the binary values (0 or 1) present at locations A, B, C, and D as indicated in the SRAM cell schematic to the right based on the inputs shown. (4 points)

A = \_\_\_\_\_  
 B = \_\_\_\_\_  
 C = \_\_\_\_\_  
 D = \_\_\_\_\_

