Points missed: _____   Student's Name: _____

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 4717 – Computer Architecture
TEST 2 for Fall Semester, 2002
Section 201

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes
- You may use one sheet of scrap paper that you will turn in with your test.
- **When possible, indicate final answers by drawing a box around them. This is to aid the grader (who might not be me!) Failure to do so might result in no credit for answer. Example:**

$$\boxed{32F1_{16}}$$

- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

"Fine print"

1. Name one benefit of memory-mapped I/O over isolated I/O. (2 points)

2. Name one benefit of isolated I/O over memory-mapped I/O. (2 points)

3. There were five functions discussed in class of an I/O module. List three of them. (3 points)

One of the ways of handling multiple interrupts was to provide a different interrupt line for each module. Answer the next two questions based on this method.

4. What is the main drawback of this method of handling multiple interrupts? (3 points)

5. What sets the priority of each interrupt with this method? (2 points)

Another way of handling multiple interrupts was through a single interrupt line with a software poll. Answer the next two questions based on this method.

6. What is the main drawback of this method of handling multiple interrupts? (3 points)

7. What sets the priority of each interrupt with this method? (2 points)

8. How is the interrupt priority set for the daisy-chain method of handling multiple interrupts? (2 points)

9. When a DMA module takes control of a bus, and while it retains control of the bus, what does the processor do? (2 points)

10. Setting up a DMA transfer required the DMA module be told four details of the transfer. What are they? (4 points)

11. Assume a processor uses three bus cycles (fetch instruction, fetch operand, store result) for each instruction, and it is executing 2×10^6 instructions per second. If a DMA that acts as a bridge between an I/O device and the system bus uses cycle stealing to store one byte to memory at the rate of 1000 bytes per second, how many instructions per second can the processor execute? (5 points)

12. Recalculate your answer to the previous question assuming the DMA and the I/O device are both attached to the system bus. (3 points)

13. Assume a serial interface is providing data at the rate of 1 Mbyte/second. The I/O module that is connected to this interface interrupts the processor each time a full byte is received. If the processor takes 250×10^{-9} seconds to service the interrupt, what percentage of time is the processor spending in the interrupt service routine? (5 points)

14. What problem is created for the processor in the previous question if the amount of time that the ISR takes exceeds 1×10^{-6} seconds? Be specific in your answer. (3 points)

Bus Architectures

15. Name two of the three drawbacks discussed in class of a single-bus architecture. (4 points)

16. What is the difference between a dedicated bus architecture and a time multiplexed bus architecture? (3 points)

17. Name two advantages of serial over parallel due to fewer wires in the bus. (3 points)

18. Name an advantage of parallel over serial. (2 points)

PCI Bus Architecture

19. Is the PCI bus a parallel or serial bus? (2 points)
20. Is the PCI bus a dedicated or time multiplexed bus? (2 points)
21. Does the PCI bus support isolated I/O? (2 points)
22. Does the PCI bus arbitration use a single arbiter or distributed arbitration? (2 points)
23. What purpose do the C/BE (bus command and byte enable signals) lines serve when valid data is on the PCI data lines? (3 points)

24. What is the purpose of the JTAG/Boundary Scan pins? (2 points)

Operating Systems

25. List and describe the two methods for resolving fragmentation in a system using dynamic partitioning. (4 points)

26. Architecture-wise, what is the main difference between paging and segmentation? (3 points)

27. Which does the application programmer have access to, paging or segmentation? (2 points)

28. What state is a process in if it is currently in the short-term queue? (2 points)

29. Will a processor still service I/O interrupts of a process in the blocked or waiting state? (2 points)

30. List the three reasons discussed in class for the need for interrupts in the scheduling portion of an operating system. (4 points)

31. List three benefits of paging over earlier systems of memory management. (4 points)

32. What problem would be caused by large page sizes? (3 points)

33. What problem would be caused by very small page sizes? (3 points)

34. Using the page table shown to the right representing a specific process, calculate the physical address from the logical address $23F5_{16}$. Assume a page size of $2^{12}=4K$. Be sure to show your work. (4 points)

1A
1C
1D
20
22
23

35. If N processes are running in paged memory, what is the largest amount of memory that is being wasted? (3 points)