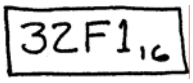
Points missed: _____ Student's Name: _____

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 4717 – Computer Architecture
TEST 2 for Fall Semester, 2003
Section 201

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes
- You may use one sheet of scrap paper that you will turn in with your test.
- **When possible, indicate final answers by drawing a box around them. This is to aid the grader (who might not be me!) Failure to do so might result in no credit for answer. Example:**



- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

Memory Management

1. Name the primary advantage of unequal-sized fixed partitions over equal-sized fixed partitions. ***Be as specific as you can be.*** (3 points)

2. Name the primary advantage of dynamic-sized partitions over unequal-sized fixed partitions. ***Be as specific as you can be.*** (3 points)

3. Name two advantages of paging over dynamic-sized partitions. ***Be specific.*** (3 points)

4. What is the theoretical upper limit on the amount of wasted memory for 10 processes in paged memory with 1K word pages? (2 points)

5. What problem is typically caused by very small virtual memory page sizes? (3 points)

6. What problem is typically caused by large virtual memory page sizes? (3 points)

7. What does a "page fault" mean in terms of virtual memory? (3 points)

8. If a process is allocated 2^{20}=1 Megabyte of virtual memory in a system where a page size is 2^{9}=512 bytes, how many potential pages would the page table require if each page table entry required 4 bytes? (4 points)

RAID

9. True or False: RAID level 0 does not provide data backup but does improve performance. (2 points)
10. Which level(s) of RAID (0 through 6) can recover from 2 drives failing at the same time? (2 pts)

11. Which level(s) of RAID (0 through 6) detects errors using an error detection scheme such as a Hamming Code? (2 points)

12. Which level(s) of RAID (0 through 6) does not provide data recovery? (2 points)

13. Assume that disk 1 of 5 total disks in a RAID 3 system fails and must be replaced. What value would you replace bit $X_1(i)$ with if $X_0(i)=1$, $X_2(i)=1$, $X_3(i)=0$, and $X_4(i)=0$. (2 points)

    a.) 1 b.) 0 c.) Cannot be determined. Need to know which disk was parity disk.

14. How is RAID level 5 an improvement over RAID level 4? (3 points)

15. RAID levels 1 and 2 share a negative characteristic. What is that characteristic? (3 points)

Input/Output

16. Name the primary advantage of interrupt driven I/O over programmed or polling I/O. (3 points)

17. Name the primary advantage of DMA over interrupt driven I/O. (3 points)

18. How is priority determined for interrupts connected to the processor where each interrupt has its own interrupt line into the processor? (3 points)

19. How is priority determined for interrupts sharing a single interrupt connected to the processor where the processor must use a software poll? (3 points)

20. Name at least one other method of connecting multiple interrupts to a processor other than multiple interrupt lines or software poll. (2 points)

21. What does the processor do while a DMA module takes and retains control of a bus? (2 points)

22. What is the benefit of having a DMA act as a bridge between and I/O device and the system bus? (2 points)

23. Assume a processor uses three bus cycles (fetch instruction, fetch operand, store result) for each instruction, and it is executing $1x10^6$ instructions per second. Assume also that a DMA and the I/O device it communicates with are both attached to the processor's system bus and that the DMA uses cycle stealing to pass data back and forth. If the I/O device is generating data at the rate of 3000 bytes per second, how many instructions per second will the processor still be able to execute? (6 points)

24. Assume a data acquisition card samples a single input channel at 100,000 samples per second, each sample being 16 bits. The interrupt service routine that receives each 16-bit sample and stores it takes 0.7 microseconds ($7x10^{-7}$ seconds) to execute. Assuming the processor can be dedicated to this operation, what is the maximum number of channels this system can handle? (6 points)

Bus Architectures

25. What is the benefit of a time multiplexed bus architecture? (2 points)

26. List two problems that occur when the number of devices on a single bus increases. (3 points)

27. List two benefits of going to a multiple bus architecture. (3 points)

PCI Bus Architecture

28. True or False: The PCI bus is an asynchronous bus architecture. (2 points)
29. True or False: The optional PCI bus lines include cache control lines to be used with multiple devices sharing memory. (2 points)
30. Is the PCI bus a dedicated or time multiplexed bus? (2 points)
31. What does the device currently controlling the bus use the FRAME bus signal for? (2 points)
32. Does the PCI bus arbitration use a single arbiter or distributed arbitration? (2 points)
33. How many parity lines are used to provide even parity across all of the address/data lines and the command/bus enable lines on the mandatory PCI signal lines. (2 points)
34. One of the purposes of the PCI bus lines C/BE is to indicate which of the four byte-lanes carry meaningful data. What is their other purpose? (3 points)

Firewire Bus Architecture

35. What is the first method a Firewire network uses to decide who gets access to the bus when simultaneous bus requests occur? (2 points)
36. What is the maximum percentage of time a high-priority node can control a Firewire bus? (2 points)
37. Which Firewire gap period is shorter, the acknowledge gap or the sub-action gap? (2 points)
38. Which form of Firewire transmission is best used for devices such as audio capture cards that regularly generate large amounts of data, asynchronous or isochronous? (2 points)
39. How often can a non-priority device control the Firewire bus during a single “fairness interval”? (2 points)