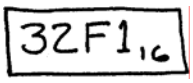
Points missed: _____ Student's Name: _____

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 4717 – Computer Architecture
TEST 2 for Fall Semester, 2006
Section 201

Read this before starting!

- The total possible score for this test is 100 points.
- This test is ***closed book and closed notes***
- ***Please turn off all cell phones & pagers during the test.***
- You may use one sheet of scrap paper that you will turn in with your test.
- When possible, indicate final answers by drawing a box around them. This is to aid the grader. ***Failure to do so might result in no credit for answer.*** Example:



- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

Data Encoding and Hard Drive Timing

1. List one of the two reasons discussed in class why data encoding is necessary to store data on a hard drive, i.e., why must a pattern of polarity changes be used to store data instead of simply having one polarity direction represent 1's while the other direction represents 0's. (2 points)

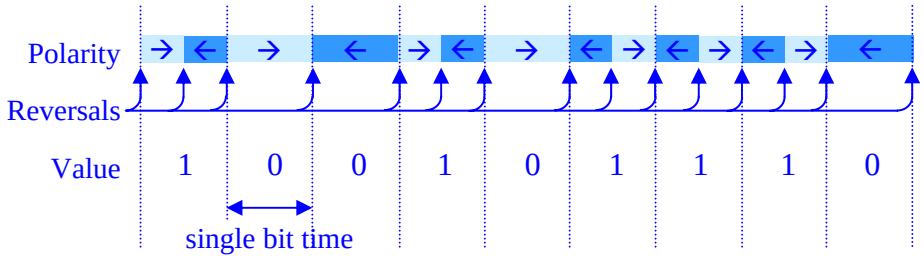
   1.) The controllers only detect changes in magnetic direction, not the direction of the field itself.
   2.) Large blocks of data that are all 1's or all 0's would be difficult to read because eventually the controller might lose track of where one bit ended and the next began.
   3.) Using a direction of polarity would force the width of a bit to equal the write head gap. Encoding can be used to compress data so that the width of a bit could be smaller than that.

2. True or false: A good encoding scheme must be backwards compatible, i.e., a newer encoding scheme should be able to read older encoding schemes. (2 points)

   Since the encoding scheme only affects the relation between the hard drive controller and its own platters and since you never swap platters, there is no need for backwards compatibility.

3. FM encoding has a magnetic polarity change at the beginning of every bit time and in the middle of a bit time representing a logic 1. Therefore, the width of 1 bit is equal to _____ times the width of the gap in the hard drive's write head. (2 points)

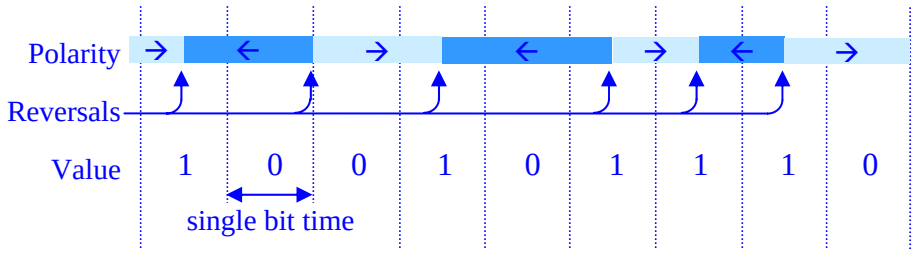
   a.) ½ b.) ¾ c.) 1 d.) 1.5 e.) 2 f.) 3 e.) varies



   From the example above, we can see that for some cases, it is necessary to have the polarity change twice within a single bit time. Therefore, the width of 1 bit must be 2 times the width of the write head gap.

4. MFM encoding has a magnetic polarity change in the middle of a bit time representing a logic 1 and between adjacent logic 0's. Therefore, the width of 1 bit is equal to _____ times the width of the gap in the hard drive's write head. (2 points)

   a.) ½ b.) ¾ c.) 1 d.) 1.5 e.) 2 f.) 3 e.) varies



   From the example above, we can see that for some cases, consecutive 1's or consecutive 0's, it is necessary to have the polarity change once within a single bit time. Therefore, the width of 1 bit must be 1 times the width of the write head gap.

5. Define "seek time." (3 points)

The time it takes to position the head over the correct track.

6. Which of the following statements best describes Rotational Position Sensing? (2 points)

☐ - Allows the CPU to query the position of the hard drive's read/write head
☐ - Informs the CPU how long the data transfer will take so it knows how long the DMA will be seizing the bus.
☐ - Used to monitor things such as spin-up time to predict hard drive bearing failure
■ - Frees the hard drive's I/O channel for use by other devices while the drive performs a seek
☐ - Uses special encoding on the hard drive's motors to identify the position of the disks

RAID

7. Assume a user needs the storage capacity of 8 hard drives. How many drives would the user need for each of the following implementations of RAID? (Note: Hamming SEC requires 4 bits to correct errors in 8-bit values.)

RAID 0 **8 – no redundancy** drives (1 point)

RAID 1 **16 – mirrored disks** drives (1 point)

RAID 2 **12 – Hamming 8 + 4** drives (1 point)

RAID 5 **9 - 1 staggered parity** drives (1 point)

RAID 6 **10 – 1 parity + 1 check** drives (1 point)

8. Does RAID 0 with its data striped across all disks in a round-robin fashion access data ***faster*** or ***slower*** than a single large hard drive? (2 points) faster

9. Which is better suited for high data storage rates, RAID 4 or RAID 5? (2 points) RAID 5

10. A RAID 1 array consisting of 6 disks could ***potentially*** survive a maximum of _____ (1, 2, 3, 4, 5, or 6) simultaneous disk failures. (2 points) 3, i.e., ½ the mirrored disks

11. Assume that disk number 1 in a RAID 3 system with 5 drives fails and must be replaced. What value would you replace bit $X_1(i)$ with if $X_0(i)=0$, $X_2(i)=0$, $X_3(i)=0$, and $X_4(i)=1$. (2 points)

(a.) 1 b.) 0 c.) Cannot determined. Need to know which disk of 5 served as parity disk.

XOR is an odd mathematical operation in that any of the terms of a sequence of XOR'ed values can be moved to the other side of the equal sign with no effect. For example, the expression below is true:

$0 = 1 \oplus 0 \oplus 1 \oplus 1 \oplus 1$

If we move the last XOR'ed value to the other side of the equal sign, we still have a valid expression, i.e., both sides of the expression now equal 1:

$0 \oplus 1 = 1 \oplus 0 \oplus 1 \oplus 1$

Therefore, it doesn't matter which disk is missing, an XOR of the remaining values should result in the data that was present on the original disk.

$X_1(i) = X_0(i) \oplus X_2(i) \oplus X_3(i) \oplus X_4(i)$

$X_1(i) = 0 \oplus 0 \oplus 0 \oplus 1$

$X_1(i) = 1$

12. Which level(s) of RAID (0 through 6) can recover from 2 drives failing at the same time regardless of which drives fail? (2 points)

    RAID 1, with its fully mirrored drives, could conceivably recover from multiple drives failing as long as the drives weren't the ones that were mirrors of each other. Therefore, ***RAID 6 is the only one that can recover regardless of which drives fail.***

Input/Output

13. In the table below, identify the responsibilities of the CPU for each of the I/O methods listed. Place a check mark in the box ***if the CPU must perform the task*** identified by the column heading. Do this for each of the four I/O methods: programmed I/O, interrupt driven I/O, direct memory access, and I/O channel. (7 points)

I/O Method	CPU initializes I/O device	CPU checks I/O device regularly to see if it needs attention	CPU handles data transfer between I/O device and memory	Requires interrupt structure in CPU
Programmed I/O	X	X	X	☐
Interrupt Driven I/O	X	☐	X	X
DMA	X	☐	☐	X
I/O Channel	☐	☐	☐	X

14. How is priority determined for interrupts that use bus arbitration to place their interrupt vector on the bus? (3 points)

    If two interrupts arrive at the same time, the arbiter decides which one is acknowledged first. Therefore, the arbiter determines the priority.

15. How is priority determined for interrupts sharing a single interrupt in a daisy chain or hardware poll configuration? (3 points)

    Remember that a daisy chain or hardware poll configuration has the interrupt daisy-chained through each device into a single interrupt input on the processor. The processor then sends an interrupt acknowledge back down a chain through the devices. Priority is set by order in which interrupt acknowledge gets to I/O modules, i.e., order of devices on the chain.

16. How many times must the DMA use the bus for a single data transfer if both the DMA module and the I/O device are both connected to the system bus? (2 points)

    a.) 1 (b.) 2 c.) 3 d.) 4 e.) None of the above

17. How many times must the DMA use the bus for a single data transfer if the DMA module acts as a bridge between the I/O device and the system bus? (2 points)

a.) 1 b.) 2 c.) 3 d.) 4 e.) None of the above

18. Assume that an interrupt service routine (ISR) is called once for each byte of data received from an analog-to-digital converter. Assume also that the ISR takes 3 microseconds (3×10^{-6} seconds) to execute. What is the maximum number of bytes per second that this system can receive from the analog-to-digital converter? You may leave your answer in the form of a mathematical expression. (4 points)

If the ISR takes 3 microseconds to process a single byte, then how many times can we execute the ISR in a second? Answering this question will tell us the maximum number of bytes per second that we can process.

$$\frac{1 \text{ second}}{3 \times 10^{-6} \text{ seconds/byte}} = 333{,}333 \text{ bytes}$$

19. How does the DMA controller inform the processor that it has completed a transfer between memory and an I/O device? (2 points)

DMA sends interrupt to the processor when it has completed the transfer.

20. Place a check in all of the boxes that truthfully complete the sentence, "An I/O Channel..." (4 points)

☐ - is the electrical connections that connect an I/O module to the I/O device
☒ - can execute a set of instructions given to it by the CPU
☒ - is an extension of the DMA concept and therefore performs the transfer of data on its own
☐ - is the bus arbiter for I/O devices

21. When using DMA, what is "cycle stealing?" (3 points)

Cycle stealing is when the DMA seizes the system bus from the CPU in order to transfer data between the I/O device and memory. It stalls any bus activity that the CPU needs to perform.

Bus Architectures

22. List one of the benefits discussed in class of a serial bus over a parallel bus. (2 points)

Below is a short list of the benefits of serial over parallel:
- The potential for "crosstalk", the signal interference between parallel data lines, is eliminated.
- Smaller connectors make portability easier and reduce the price of the cables.
- Fewer connections are more reliable.

23. List two of the three problems discussed in class that occur when the number of devices on a single bus increases. (3 points)

- An increased number of devices usually requires a physically longer bus. A long bus causes attenuation of the bus signals and problems with signal reflections.
- Slower devices will dictate the maximum speed of the bus.
- More devices trying to communicate on the bus will cause congestion and force devices to wait longer for access to the bus.

24. What component of the system usually acts as a bridge between the processor and the system bus? (2 points)

    I accepted both cache and Northbridge as valid answers to this question.

25. One of the advantages of multiple busses was the ability to group devices of similar speeds. Name another advantage. (3 points)

    - Isolates the processor-to-memory traffic from I/O
    - Supports a wider variety of interfaces by having multiple buses
    - Higher speed devices can be placed closer to the processor preventing slower devices from interrupting their transfers.

26. In the mezzanine approach, high-speed devices are usually connected to a bus that is ***closer to*** or ***farther away*** from the processor? (2 points) ___closer to_____

27. True or false: In the mezzanine approach, slower busses are usually connected to the processor through the higher speed buses. (2 points)

28. True or false: Time multiplexed parallel busses have pins that serve more than one function. (2 points)

29. What type of bus is used to connect the Northbridge to the Southbridge in the Pentium architecture? (2 points)

    PCI

30. What signal does a bus with synchronous timing require that asynchronous does not? (2 points)

    A clock signal

PCI Bus Architecture

31. PCI commands such as those identifying the type of transaction are sent across the bus using the _____ lines. (2 points)

    a.) JTAG b.) FRAME c.) AD d.) IRDY e.) C/BE f.) None of the above

32. PCI uses address and data multiplexed onto the _____ lines. (2 points)

    a.) JTAG b.) FRAME c.) AD d.) IRDY e.) C/BE f.) None of the above

33. PCI uses _____ lines to indicate which of the four byte-lanes carry meaningful data address and data. (2 points)

    a.) JTAG b.) FRAME c.) AD d.) IRDY e.) C/BE f.) None of the above

34. The _____ lines on a PCI bus are used for testing during manufacturing. (2 points)

    a.) JTAG b.) FRAME c.) AD d.) IRDY e.) C/BE f.) None of the above

35. Does the PCI bus arbitration use a ***single arbiter*** or ***distributed arbitration***? (2 points) ___single arbiter___

Of the following characteristics, identify by placing a checkmark in the appropriate column whether the characteristic describes PCI, PCI-X, and/or PCI-E. Some rows (characteristics) will have more than one checkmark. (Each row is worth 2 points)

Characteristic	PCI	PCI-X	PCI-E
Parallel bus structure	☒	☒	☐
Uses differential signalling similar to Manchester encoding to allow for long distance communication	☐	☐	☒
Standard supports 1, 2, 4, 8, 16, or 32 serial lanes for devices to communicate across	☐	☐	☒
Which is ***physically*** backwards compatible with PCI? (Check either PCI-X or PCI-E)		☒	☐
Supports the PCI command structure making it compatible with legacy software. (Check one or both)		☒	☒
Which is the fastest? (Check one)	☐	☐	☒