

Points missed: _____ Student's Name: _____

Total score: _____ /100 points

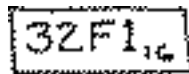
East Tennessee State University
Department of Computer and Information Sciences
CSCI 4717 – Computer Architecture
TEST 3 for Fall Semester, 2002

Section 201

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes
- You may use one sheet of scrap paper that you will turn in with your test.
- **When possible, indicate final answers by drawing a box around them. This is to aid the grader (who might not be me!) Failure to do so might result in no credit for answer.**

Example:



32F1,6

- **1 point will be deducted** per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.

“Fine print”

Academic Misconduct:

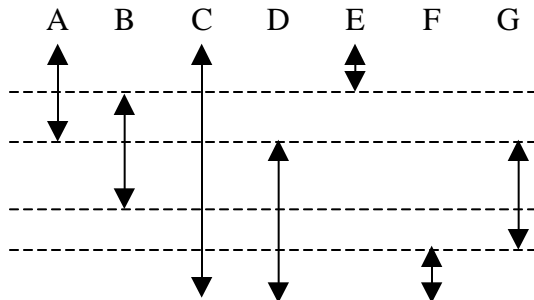
Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing or falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

Short answers – Each answer is worth 2 points

1. In relative addressing, the operand specifies an address relative to _____.
2. Identify the following operands as immediate (I), direct (D), indirect (N), register (R), register indirect (G), displacement (S), relative (L), or indexing (X) addressing.
_____ Constant
_____ Pointer to an array with an offset indicating values inside the array
_____ Operand is an address pointing to a limited address space
_____ Combines direct addressing and indirect addressing
_____ A register contains the address which in turn contains the data
3. Assume 5 instructions with no branches are passed through a pipeline with 6 stages. Using Δ to represent the time it takes to complete a stage, how long will it take to pass all 5 instructions through the pipeline?
a.) 5 c.) 10 e.) 12 g.) 14
b.) 8 d.) 11 f.) 13 h.) None of the above
4. Assume that the third instruction of the five instructions from the previous questions is a conditional branch that results in a branch. If the processor prefetches the branch target, how long will it take to pass all 5 instructions through the pipeline?
a.) 10 c.) 12 e.) 14 g.) 16
b.) 11 d.) 13 f.) 15 h.) None of the above
5. For a 3 stage pipeline, as the number of consecutive instructions without a branch goes to infinite, the speed up factor over a non-pipelined processor is:
a.) 2 b.) 3 c.) 4 d.) 6 e.) 9 f.) None of these
6. If three bits are used for each branch instruction in a branch history table, then the branching results for the last _____ occurrences of the instruction can be maintained.
a.) 2 b.) 3 c.) 4 d.) 6 e.) 8 f.) None of these
7. If a single bit is used for a branch history and it is initialized to the "don't branch" state, then how many erroneous predictions will be made during the execution of a typical loop?
a.) 1 b.) 2 c.) 3 d.) Varies depending on the circumstance
8. True or false: The branch history bits are typically stored in main memory with the code.
9. True or false: The delayed branch method of handling branches with a pipeline does not require the pipe to be flushed.
10. If a processor has eight register windows forming a circular stack, how many function calls can be present at one time. (Include the top-level function in your count.)
a.) 3 b.) 4 c.) 5 d.) 6 e.) 7 f.) 8 g.) 9

11. What mechanism is used (i.e., what function of the processor handles the operation) if the code runs out of register windows and needs to store data to memory?
12. For the time sequence of variables shown in the figure below, what is the minimum number of registers that will be needed to run this code without having to store any data to memory?



(Arrows represent time that variable is active)

- a.) 3 b.) 4 c.) 5 d.) 6 e.) 7 f.) 8 g.) 9
13. Is the directory protocol for cache coherence in multiprocessor systems central or distributed control?
14. Assume a multiprocessor system uses the MESI protocol. If the current state of a line in processor A's cache is shared and processor B modifies that data without writing the new value to main memory, what does the state of that line in processor A's cache change to?
 - a.) modified b.) exclusive c.) shared d.) invalid e.) cannot be determined
15. Assume a multiprocessor system uses the MESI protocol. If the current state of a line in processor A's cache is shared and processor A modifies that data without writing the new value to main memory, what does the state of that line in processor A's cache change to?
 - a.) modified b.) exclusive c.) shared d.) invalid e.) cannot be determined
16. Assume a multiprocessor system uses the MESI protocol. If processor A contains a line in its cache that no other processor contains in its cache, what is the state of the line in processor A's cache?
 - a.) modified b.) exclusive c.) shared d.) invalid e.) cannot be determined
17. Assume a multiprocessor system uses the MESI protocol. If a processor modifies data that is in the exclusive state, is it required to update main memory?
18. For the following code, how many virtual registers will need to be created using register renaming? Do not count the original assignment of register values.

```

R3 ← R3 + R5
R5 ← R3 + 1
R3 ← R3 + R5
R5 ← 5
R3 ← R3 + R5

```

Answer: _____

19. Which of the following dependencies requires that data be read before it is overwritten?
a.) true data dependency b.) output dependency c.) antidependency
20. Which of the following dependencies requires a new data value be written before it is read?
a.) true data dependency b.) output dependency c.) antidependency
21. Which of the following dependencies indicates that data could be written out of order?
a.) true data dependency b.) output dependency c.) antidependency
22. The snoopy protocol is more suited to the _____ interconnection method for symmetric multiprocessors.
a.) time-shared bus b.) multiport memory c.) central controller

Medium answers – Each answer is worth 5 points

23. Aside from a branching instruction, name two other situations that might force a pause in the stages of a pipeline. Do not list any of the issues associated with superscalar machines.

24. In class, we addressed a number of problems related to using two pipelines or streams to handle conditional branches so that both the non-branching and branching streams could be in a pipeline. Name two of the problems.

25. Smaller programs result in less memory being required. Name another advantage of smaller programs discussed in class?

26. Name four specific characteristics that differentiate CISC and RISC processors.

27. What is the purpose of adding NOOPs after branches and loads in the assembly language code of a RISC processor?

28. Describe the operation of and give a real-world application of Single Instruction, Multiple Data Stream (SIMD) multiprocessing.
29. List three characteristics of a symmetric multiprocessor architecture.
30. Name one advantage and two disadvantages of the multi-port memory interconnection method for symmetric multiprocessors over the time shared bus.
31. The code below uses a three-operand instruction. In the space below you will write three short programs that do exactly the same thing, one with two-operand instructions, one with one-operand instructions, and one with zero-operand instructions. If it fits the need of the instruction, feel free to use register names R1, R2, etc.

```
ADD destination, source1, source2
```

| Two operand instructions | One operand instructions | Zero operand instructions |
|--------------------------|--------------------------|---------------------------|
| | | |

32. The code on the right is a modification of the CISC code on the left for the purpose of using on a RISC processor. Are the two pieces of code going to operate the same on their respective processors? If not, why?

```
MOV    R1, MEM
MOV    R2, 0
ABC    SUB   R1, 10
      INC   R2
      CMP   R2, 100
      BEQ   EXIT
      JMP   ABC
```

```
MOV    R1, MEM
MOV    R2, 0
      SUB   R1, 10
ABC    INC   R2
      CMP   R2, 100
      BEQ   EXIT
      NOOP
      JMP   ABC
      SUB   R1, 10
```