CS/EE 6710 Digital VLSI Design
CAD Assignment #4
Due Thursday September 28th, 5:00pm

Overview: In this lab you'll explore the DC characteristics of transistors and some power and delay properties of collections of transistors. The material for this assignment is in Chapters 2 and 4 of the text. You'll also do a few problems from the book.

DC Analysis: The SpectreS simulations that you've done up until now in the class have been transient analysis. That is, you are applying a time-varying signal to the circuit and you're getting a simulation of the time-varying output of the circuit in response to that input. This is valuable stuff, and is generally what digital designers are mostly concerned about since this relates to the timed operating behavior of the digital circuit. However, when we're looking at the behavior of the devices themselves, we may want to do a DC analysis that looks at the steady state instead of the time-varying state. For example, Figure 2.7 in your text is a plot of steady state behavior of an nMOS transistor mapping the Ids current as Vds is changed. In fact, there are five different DC analyses in this figure. Each of the five curves is a DC analysis that holds the Vgs at a fixed level, then sweeps the Vds from 0v to 5v and plots the resulting Ids.

Chapter 6, Section 6.4 in the Lab Manual describes how to run exactly the same simulation in SpectreS. Check that out and do the following…

Problems:

1. Run a parametric DC analysis of a single nmos device as described above. The nmos device should be 1.5u wide and 0.6u long. Plot the results. Hand in schematic and output plot. Use five curves with Vgs being 1, 2, 3 , 4, and 5 volts.
2. Run a similar parametric DC analysis of the same nmos device but make it 6u wide and 0.6u long. Plot the results (five curves). How do the Ids currents compare to the 1.5u wide case? Hand in output plot only.
3. Use DC analysis to plot the switching point of a standard inverter. See Figure 2.26 in your text for an example. The inverter should be a 2x inverter with an nmos device 3u wide and a pmos device 6u wide. Connect the input to the inverter to a vdc voltage source and sweep the dc voltage from 0 to 5 volts for the DC analysis. Plot the output voltage. Hand in schematic and output plot.
4. Now change the width of the pmos device by using a variable in the width field of the pmos device and running a parametric DC analysis with five different values of the width (sweeping the input from 0v to 5v on each DC analysis). See figure 2.26 in your text for an example. Change the pmos device width from 1.5u to 7.5u in five steps. Plot the output. Which curve has the switching point closest to Vdd/2? Hand in output plot only.

5. Solve the following problems from your book: 1.14 (a,b, c only), 1.16 (a,b,c), 1.17, 2.2, 2.3, 2.10, 2.11, 2.21, 2.22