CS/EE 6710 Digital VLSI Design
CAD Assignment #7
Due Tuesday October 24th, 5:00pm

Overview: In this assignment you will, as a group, augment your library with a few simple, but important, cells, use your library to synthesize a slightly larger example, and place and route that example using the SOC Encounter place and route tool.

Procedure:

1. Augment your library with the following cells. This means creating layout, cmos_sch, symbol, behavioral, extracted, analog_extracted, and abstract views, along with .lib, .lef, and .v information. Add these cells to your UofU_6710Lib library.
   a. **INVX4** – an inverter with 4x drive
   b. **INVX8** – an inverter with 8x drive
   c. **BUF4X** – a non-inverting buffer with 4x drive. This is just a series of two inverters with the first being a 1x and the second being a 4x
   d. **BUF8X** – a non-inverting buffer with 8x drive. The first inverter should be a 2x and the second an 8x inverter.
   e. **NANDX2** – a NAND gate with 2x drive

2. Now use your new UofU_6710Lib library to synthesize the **controller** state machine from the mips example in your book. The **controller.v** behavioral file is in **/uusoc/facility/cad_common/local/class/6710/examples**. Use a target speed of a 5ns clock period for your synthesis. Look at the report file to see if you were able to hit that target speed according to Synopsys.

3. Now place and route the structural file (**controller_struct.v**) using SOC Encounter. See Chapter 10 in the CAD Manual for details. Use your buffer cells (footprint buf) as your clock-tree synthesis cells. You should end up with a correctly placed and routed circuit with no geometry or connectivity errors, and with (at least) the following files as a result
   a. **controller_soc.v** – the structural file from SOC Encounter which includes the generated clock tree and the optimizations.
   b. **controller.def** – the design exchange format (DEF) file that describes the placed and routed circuit
   c. a report file for the final post-route optimization which shows whether the placed and routed circuit met the 5ns timing.
   d. A **routed.enc** file which saves the SOC state of the final placed and routed circuit.

4. Now read the **controller.def** file back into icfb (See CAD Chapters 8 and 10 for details).
   a. Make a new library named **control**
   b. Import the **controller.def** file to this library as a layout view. Replace the abstract cells with layout cells and run DRC and Extract
   c. Import the **controller_soc.v** file (the structural Verilog file of the final placed and routed circuit from SOC) in as a schematic and symbol view
   d. Compare the schematic and extracted views with LVS and verify that they are the same.

What to turn in:

1. Tar and handin electronically the following directories:
   a. **UofU_6710Lib** – your library directory
   b. A copy of your **UofU_6710Lib.lib**, **.lef**, **.db**, and **.v** files. These can be put in your UofU_6710Lib library directory if you like.
   c. **control** – the icfb library you used to read in the controller layout and schematic
   d. **soc/control** – the directory you used when you ran SOC Encounter. This directory should include (at least) the structural Verilog file from synopsys, the structural Verilog file from SOC, and the controller.def file from SOC and the SOC saved file called routed.enc that saves the final state of your placed and routed design.
2. Print and hand in physically*:
   a. Your LVS log showing that the layout and the schematic (both produced by SOC Encounter) match
   b. The timing report from Synopsys synthesis
   c. The post-Route timing report from SOC Encounter