CS/EE 6710 — Digital VLSI Design

Pre-Requisite Review: Review of digital design

Due Friday, September 1st, 2006

Name:

Instructions

This is a takehome assignment, but it has been given in the past as a closed-notes quiz. I want to see what you remember about the prerequsite material in digital design. It should help you determine if you have the right background for this course.

Work independently. Show your work! Answers with no justification will not be given credit. *Don't Panic!*

Put your name at the top of each sheet of the exam before you start!

1 - Electronics	20 points	
2 - Arithmetic	20 points	
3 - Combinational Logic	20 points	
4 - timing	20 points	
5 - State machine design	20 points	
Total	100 points	

1 Basic Electronics

1.1 RC Circuits: 10 Points

Consider a switch that connects a 120v source, a 23 MΩ resistor, and a $5\mu F$ capacitor. How long should you leave the switch closed in order to charge the capacitor to 12v? Draw the circuit, set up the equation and solve for seconds.

1.2 Power: 10 Points

What is the maximum voltage that can be connected across a series combination of a 180Ω 2-watt resistor and a 120Ω 1-watt resistor with exceeding either resistor's power rating.

2 Arithmetic: 10 Points

Compute the following additions assuming the numbers are 2's complement numbers. Show the result, and indicate which, if any, cause overflow.

```
A)  10111001      B)  01011101      C)  00100110
  + 11010110        + 00100001        + 01011110
  ----------        ----------        ----------
```

```
D)  01001010      E)   10010110
  + 11110110         + 01001101
  ----------         ----------
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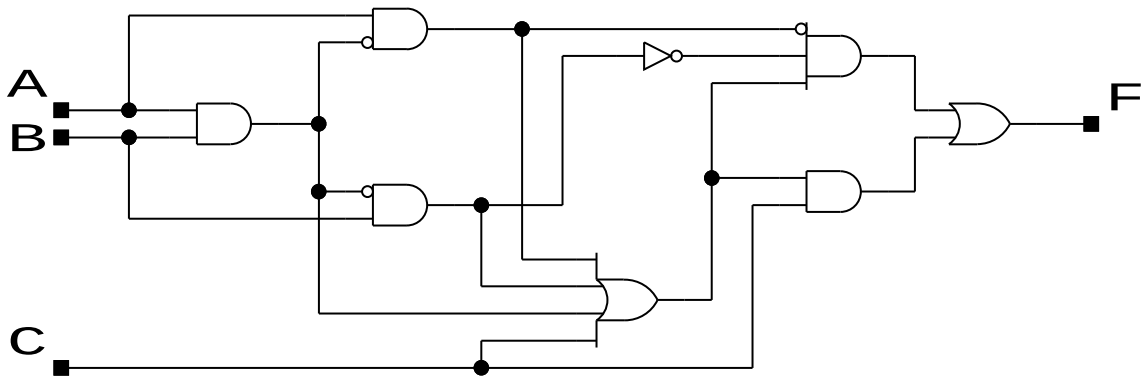
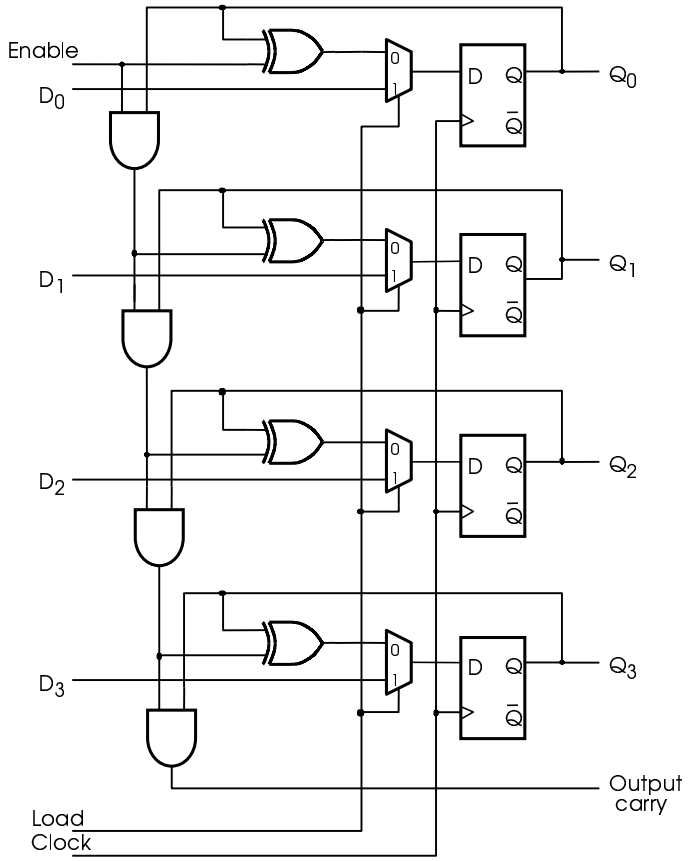
3 Combinational Logic: 10 Points

Convert the following circuit to an equivalent circuit that uses only NAND gates. Do NOT minimize the circuit, just change the gate types. Remember that using deMorgan's theorem $\overline{A \wedge B} = \overline{A} \vee \overline{B}$ which means that you can draw a NAND as an AND with inverted output or as an OR with inverted inputs.



4 Circuit Timing: 20 Points

Consider the counter circuit in the following figure (This is a synchronous counter with parallel load). Assume that T_{su} (setup time) is 3ns and T_h (hold time) is 1ns for the flip flops.
Assume that T_{pd} (propogation delay) through each gate (AND, XOR, and MUX) is 1ns.
What is the maximum clock frequency for which the counter will operate correctly? Why?



5 Finite State Machine Design: 20 Points

Design a finite state machine with one input I, and two outputs Z and E. The machine should produce a Z output whenever it has seen a 110 pattern on the input stream, except that if it ever sees a 001 pattern on the input stream, it should assert the E output, and keep that E output asserted until the machine is reset. Note that Z should never be asserted again once E is asserted. Design a state machine to implement this function. Don't implement the circuit, just draw the state diagram for a Moore-style state machine (i.e. outputs are determinied only by which state you're in).